

MODEL NAME : *Echo 15 17 nVidia*

PCB NO : *LAB752P*

BOM P/N : *4319UA31L01 / 4319UA31L02 for NV*
4319UB31L01 for AMD

Compal Confidential

Echo 15 17 with nVidia GFX

Schematic Document

Broadwell H-type

Rev: 0.1(X00)

2014/01/02

@ : Nopop Component

EMC@ : EMI part

ESD@ : ESD part

RF@ : RF part

CONN@ : Connector Component

BDW@ : Intel BOARDWELL

AOAC@ : Intel AOAC

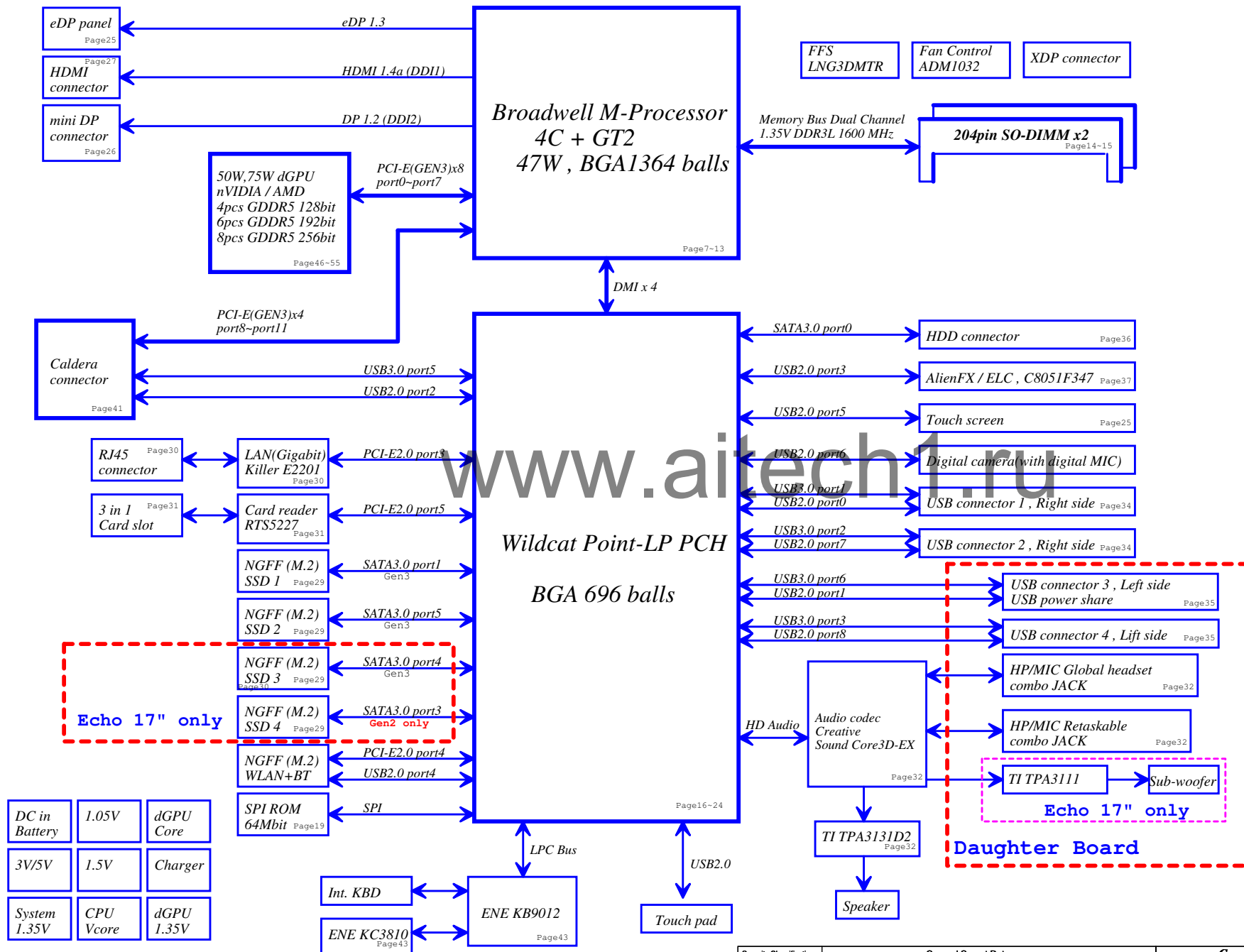
DIS@ : Discrete Part

NV@ AMD@ : Board ID

ZZZ1 PCB
DAB0000P000
PCB 18F LA-B752P REV0 M/B 8
12L

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				Sheet	1 of 69
				Rev	0.1

Echo 15"/17" Block Diagram

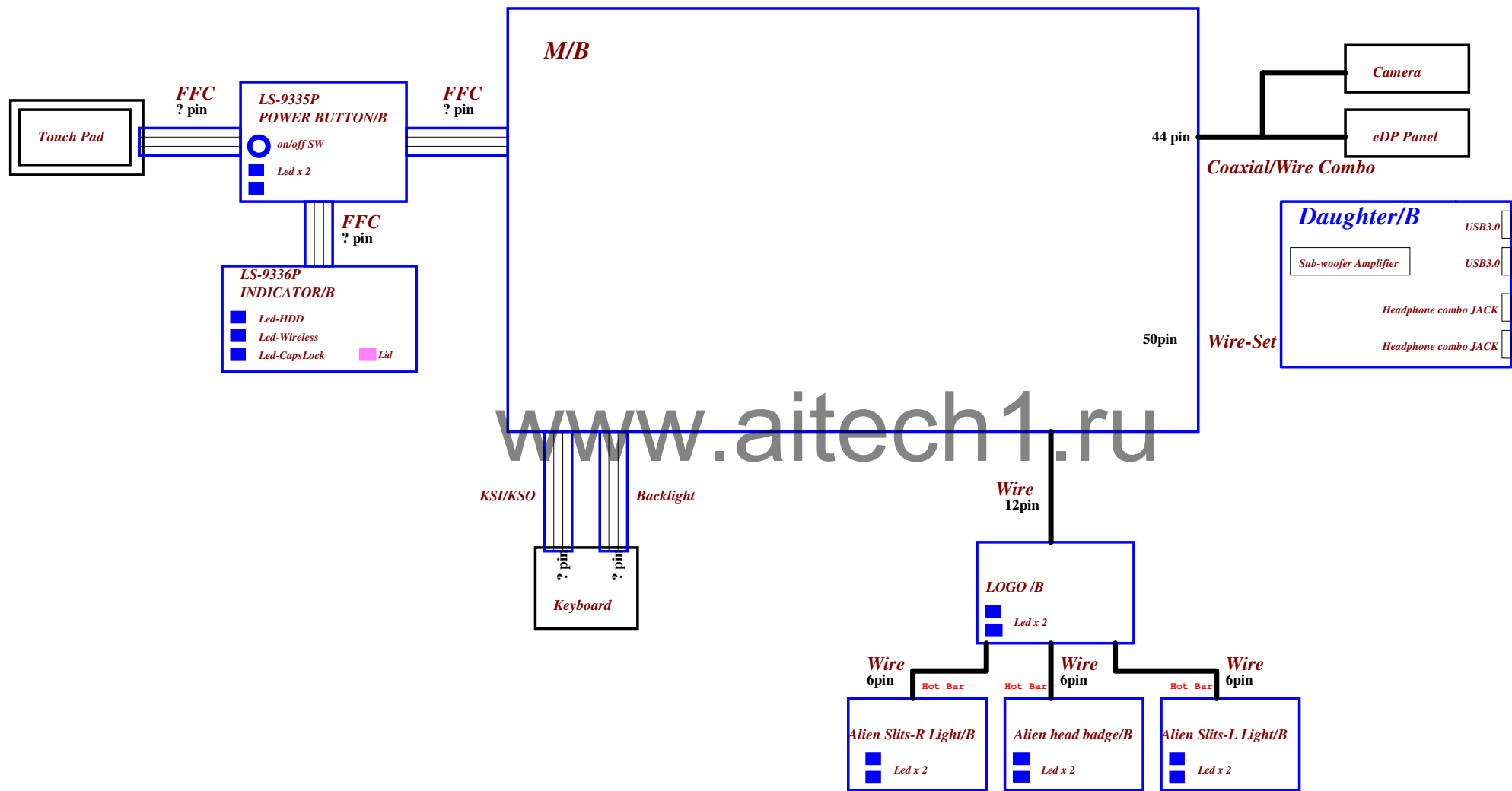


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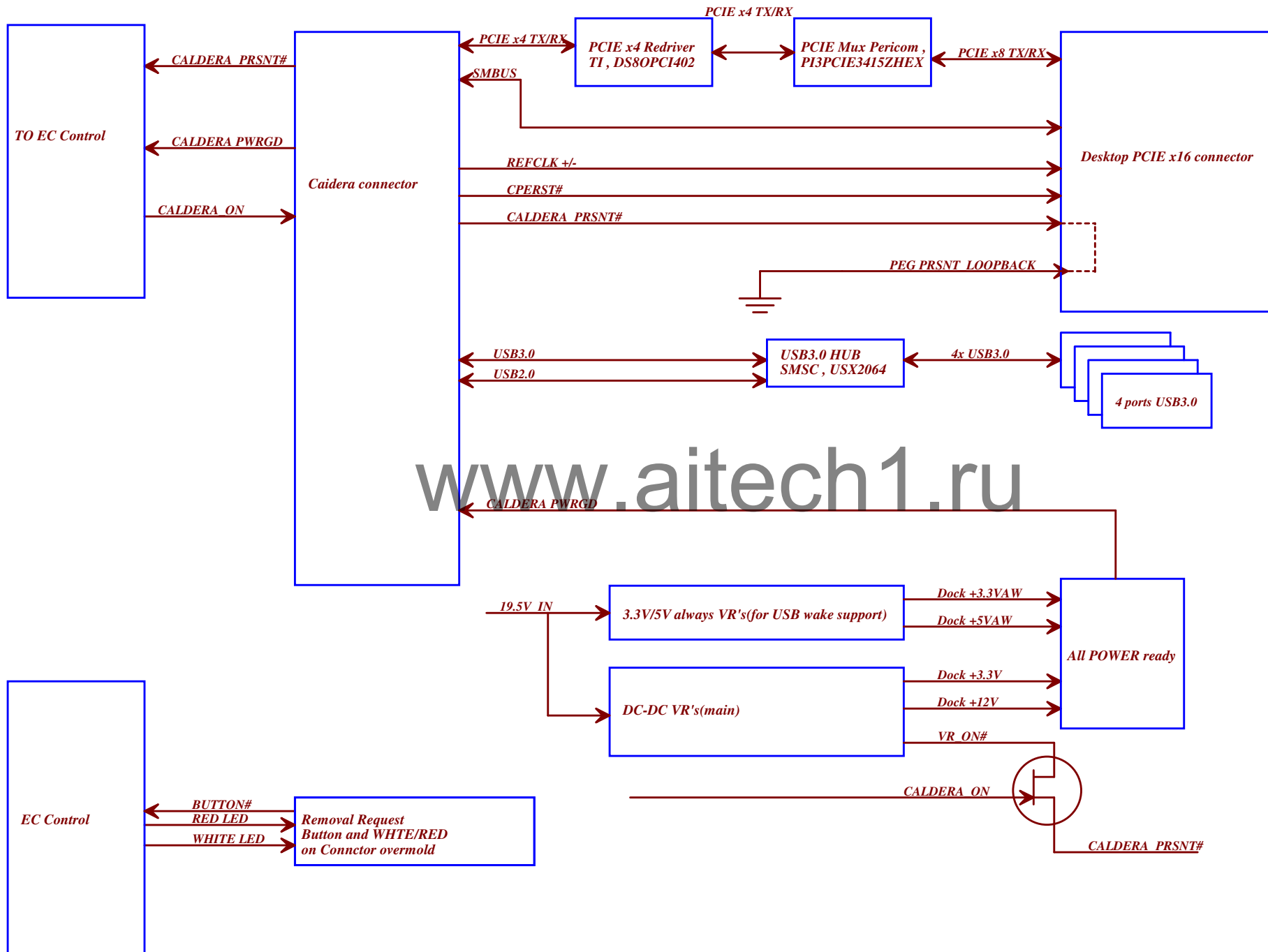
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Project Code : AAP10/AAP20

File Name : LA-XXXXP



Caldera(Echo graphic expander) block diagram



Board ID Table for AD channel

Vcc	3.3V +/- 1%					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	NVIDIA Graphic
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	AMD Graphic
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE	
19	NC	3.000V	3.300V	3.300V	0xEE - 0xFF	

Board ID TABLE

ID		PCB Revision
NV	AMD	
0	10	EVT-1
1	11	DVT-1
2	12	DVT-2
3	13	MP

Symbol Note :

 : means Digital Ground

 : means Analog Ground

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CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N15P)
CLKOUT_PCIE5	DGPU (Caldera)

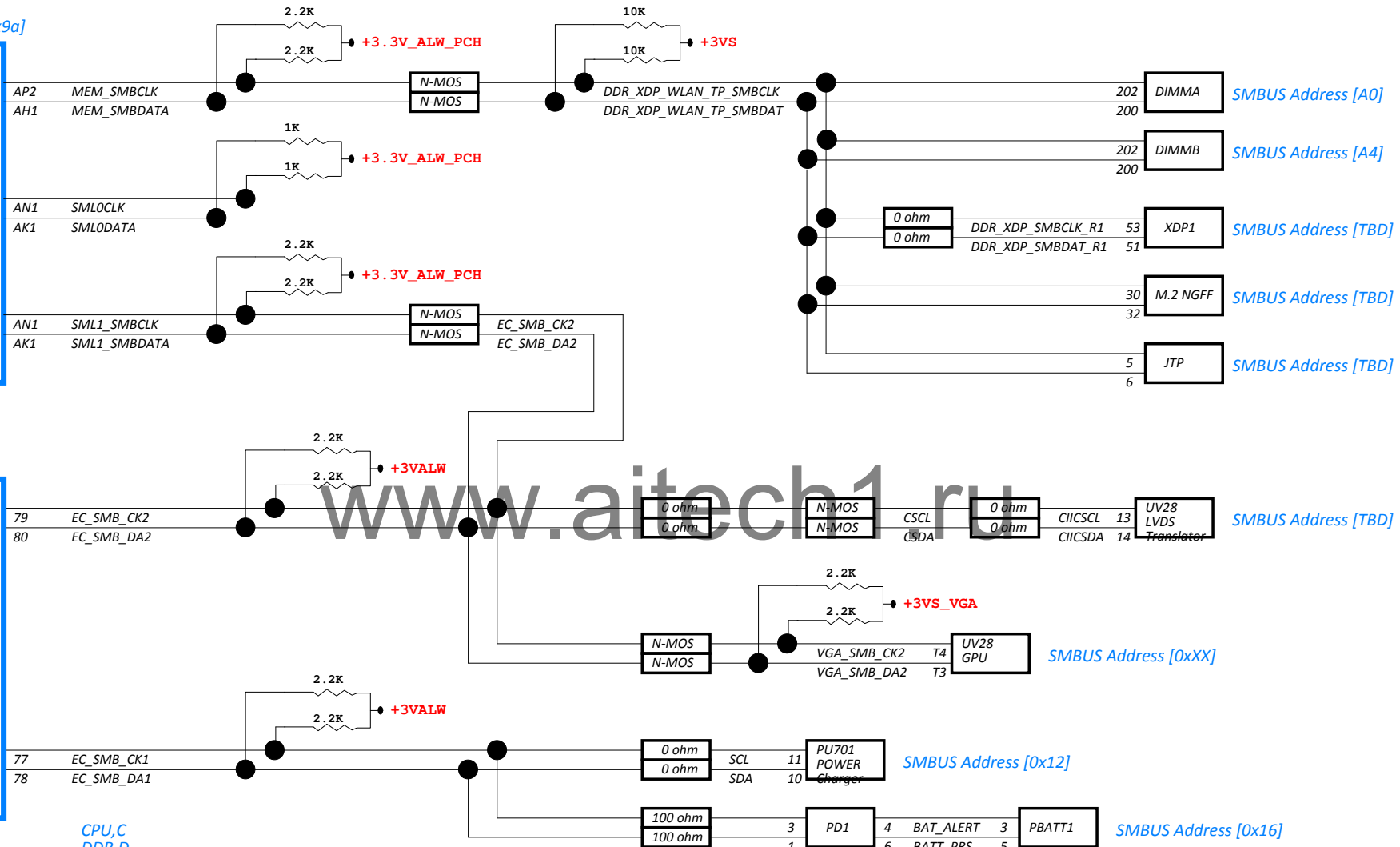
USB3.0	
Port1	Right side1
Port2	Right side2
Port3	Left side 1
Port4	
Port5	Caldera
Port6	Left side 2
USB2.0	
Port0	Right side1
Port1	Left side 1 (PowerShare)
Port2	Caldera
Port3	ELC
Port4	BT
Port5	Touch screen
Port6	Camera
Port7 / 8	Right side 2 Left side 2
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	M.2 Card WLAN
Lane 5	PCIE 4x MUX
Lane 6	
SATA	
SATA0	HDD
SATA1	NGFF SSD
SATA2	NGFF SSD
SATA3	

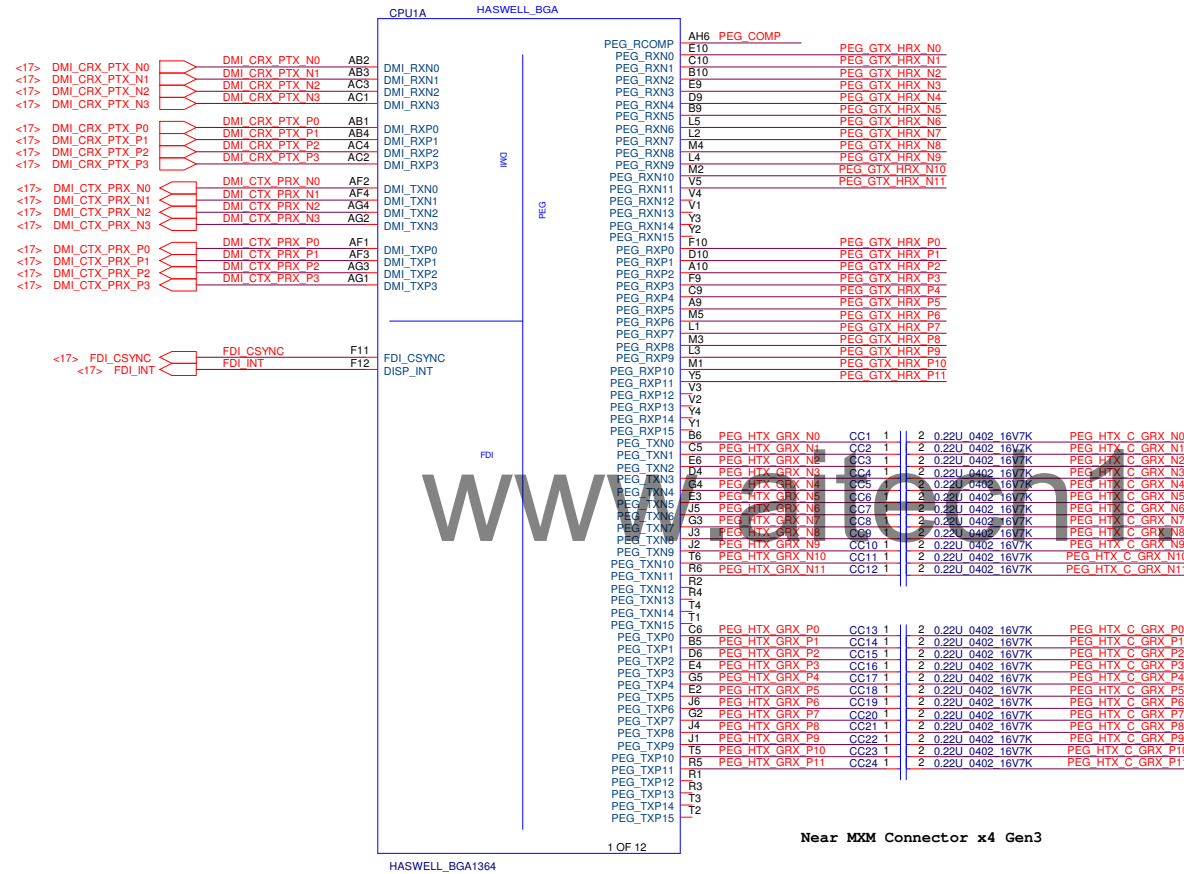
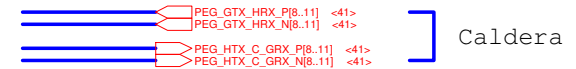
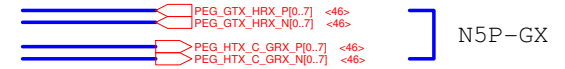
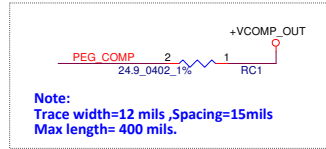
SMBUS Address [0x9a]

Broadwell

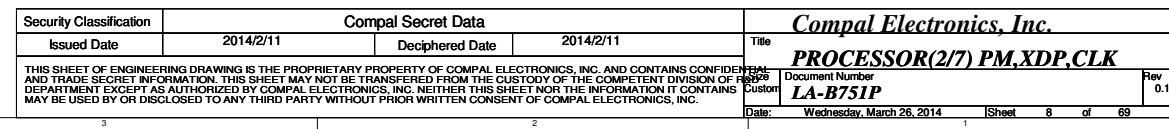
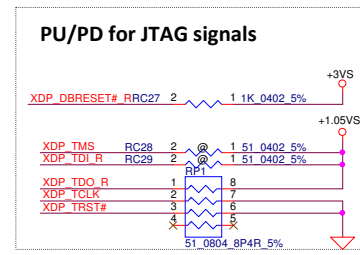
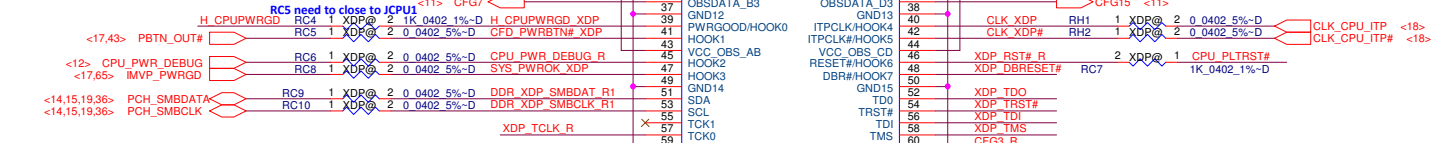
KBC
KB9012A4

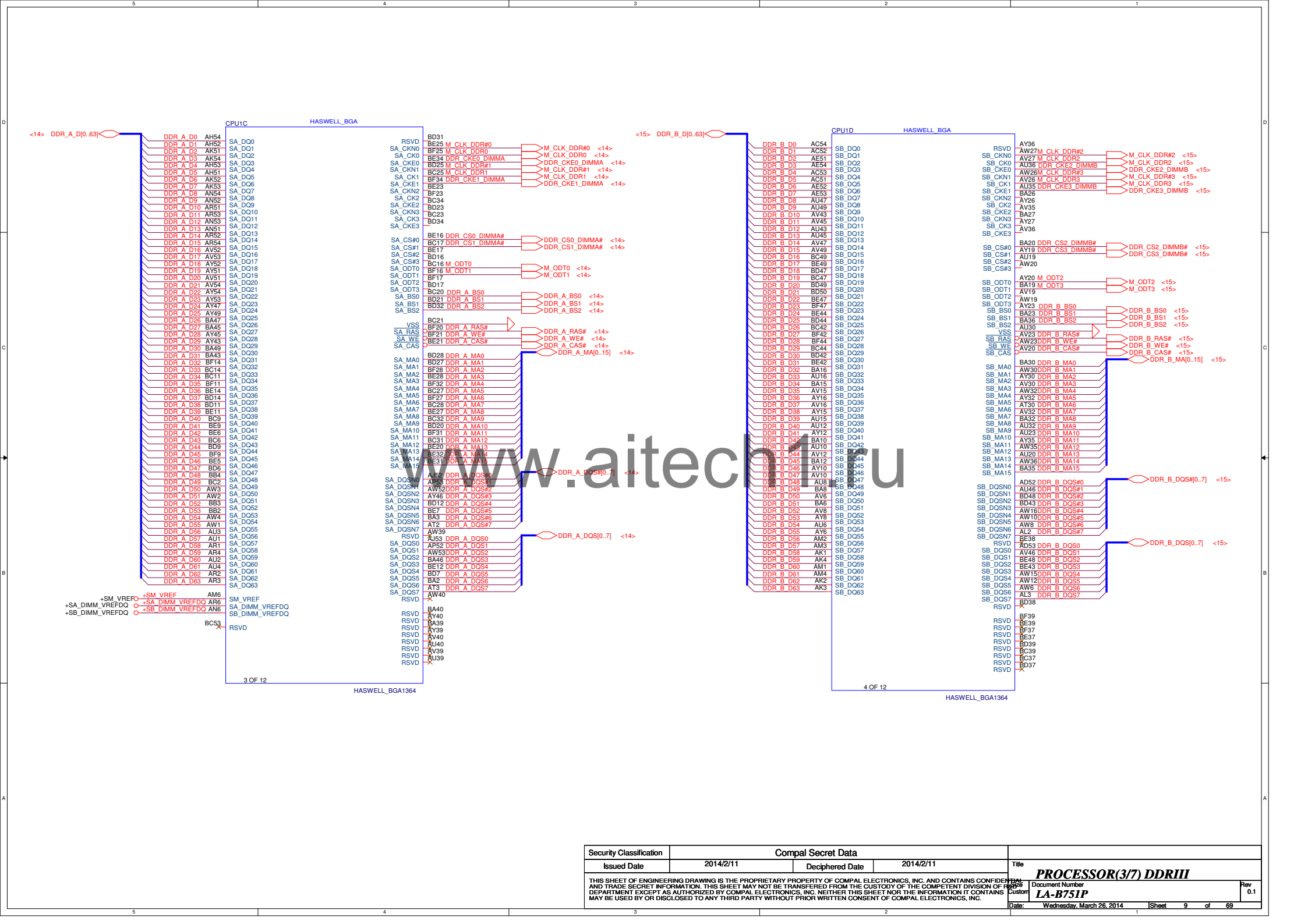
CPU,C
DDR,D
GPU,DP,HDMI,EDP,V
LAN,L
AUDIO,A
NGFF,N
USB,U
CALDERA,M
HDD,S
ELC,E
FAN,F
TP,T
KBC,K
DC,O

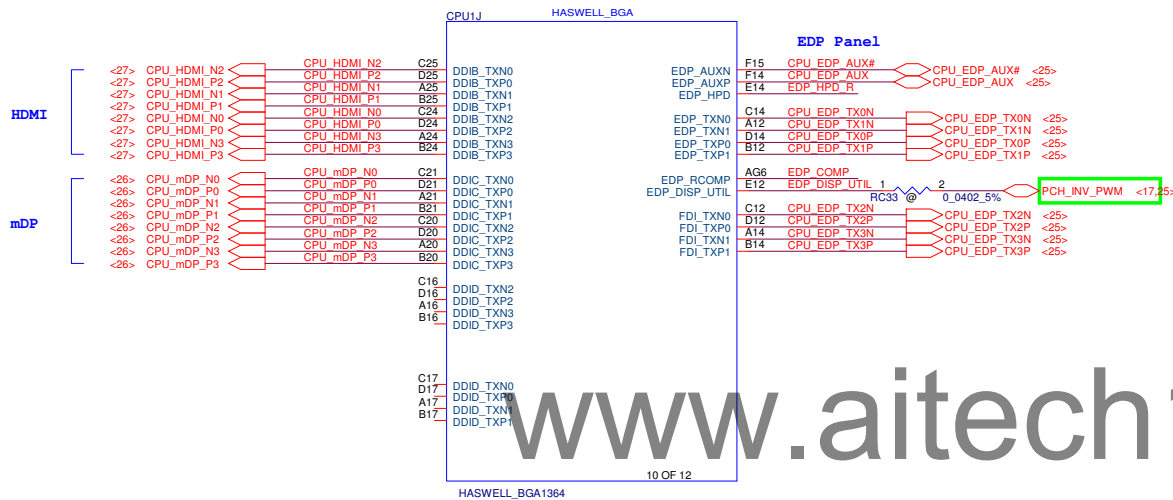




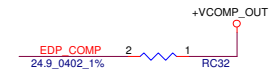
Near MXM Connector x4 Gen3





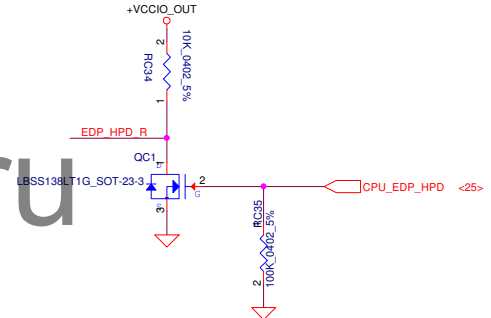


COMPENSATION PU FOR eDP



Note:
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

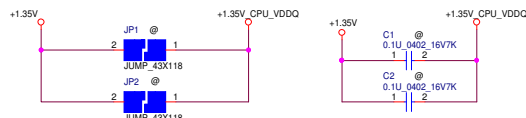
HPD INVERSION FOR EDP



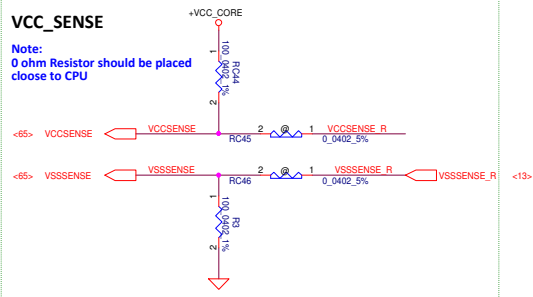
HPD is a active-high signal from device.
The HPD processor input is
active-low signal.

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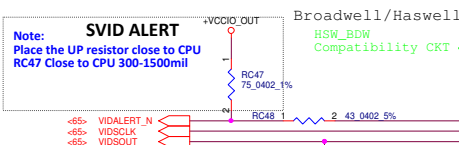
Note:
Intel Shark Bay
Removed the S3 power reduction circuit.



Note:
0 ohm Resistor should be placed
close to CPU

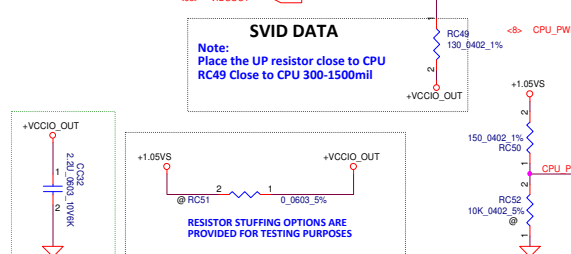


Note: **SVID ALERT**
Place the UP resistor close to CPU
RC47 Close to CPU 300-1500mil

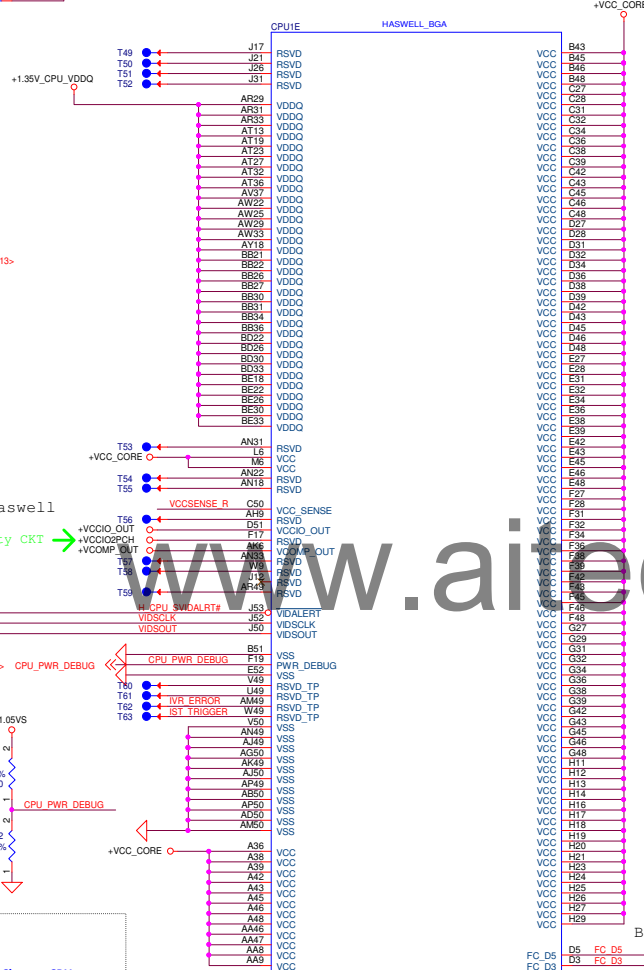
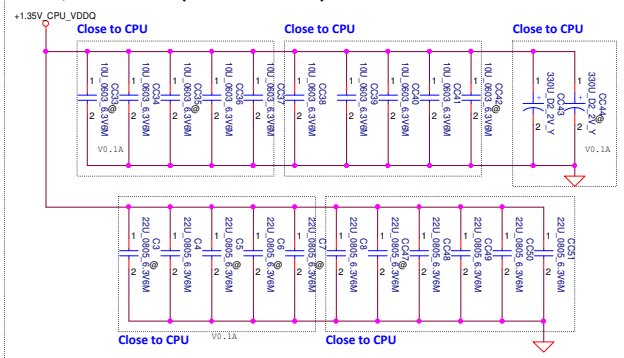


SVID DATA

Note:
Place the UP resistor close to CPU
RC49 Close to CPU 300-1500mil

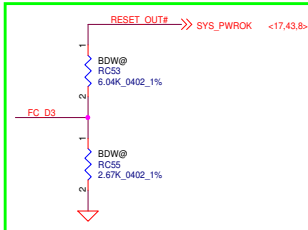


+1.35V CPU_VDDQ

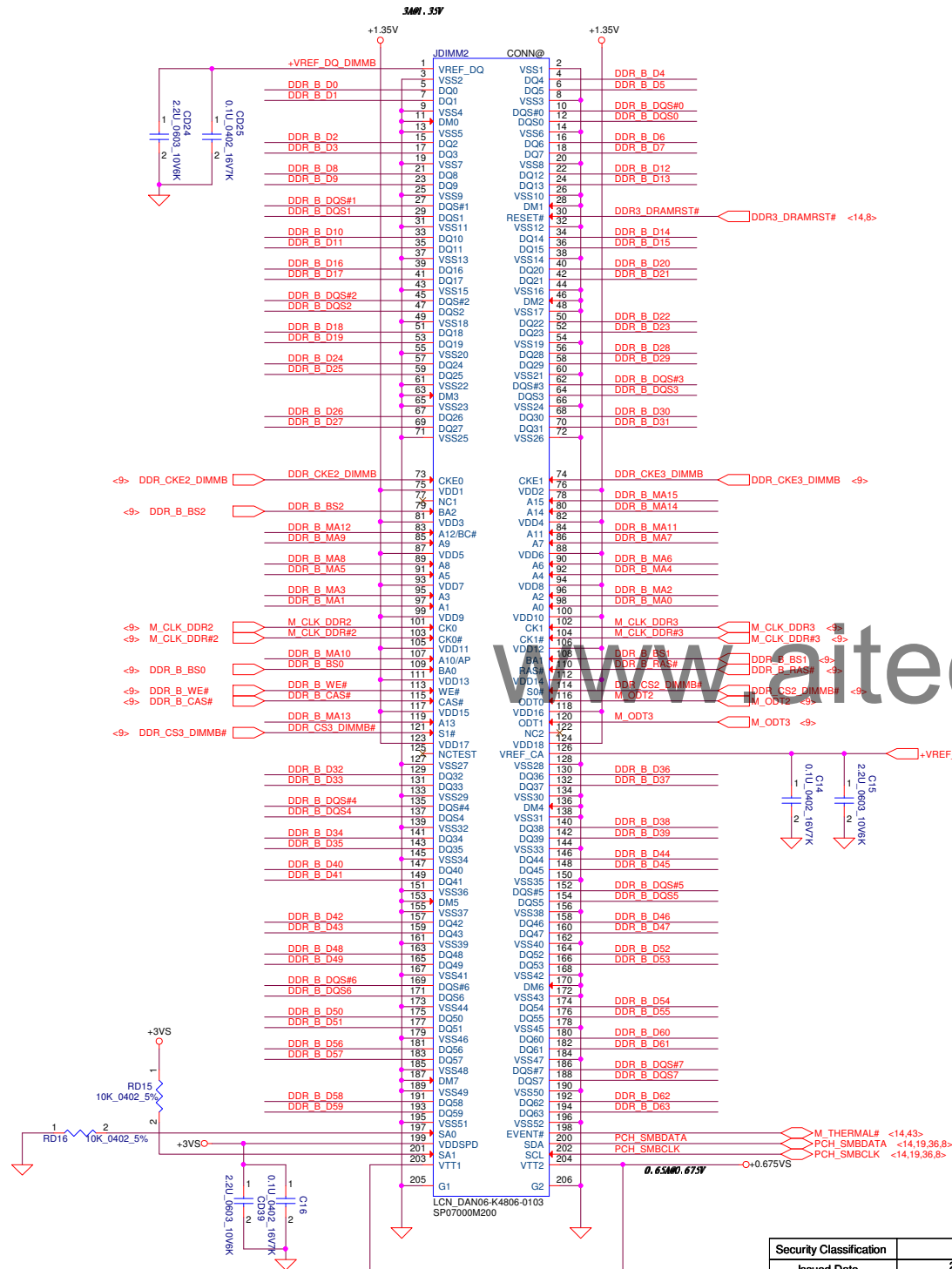


	HSW	BDW
RC54	X	V
CC45	X	V
CC46	X	V
RC53	X	V
RC55	X	V

RESET OUT#

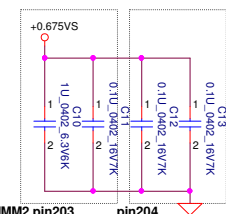


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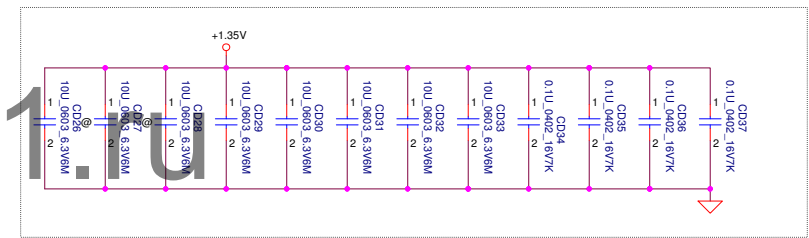
<9> DDR_B_D[0..63]
 <9> DDR_B_DQS[0..7]
 <9> DDR_B_DQS[0..7]
 <9> DDR_B_MA[0..15]

Layout Note:
Place near JDIMM2

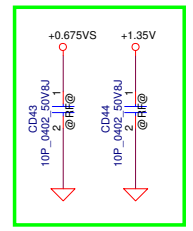


Place near JDIMM2 pin203

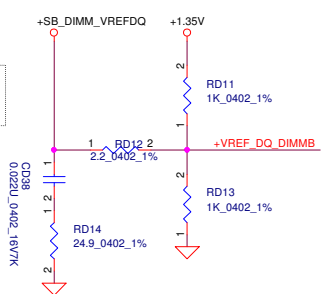
Layout Note:
Place near JDIMM2



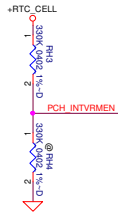
Layout Note:
Place near JDIMM3



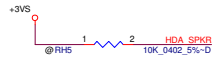
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes



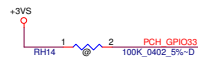
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INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
High - Enable Internal VRs
Low - Enable External VRs



NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH

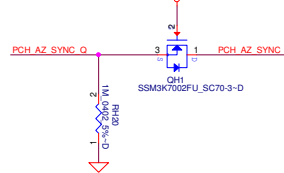


FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DISABLED (DEFAULT)
HIGH = ENABLED

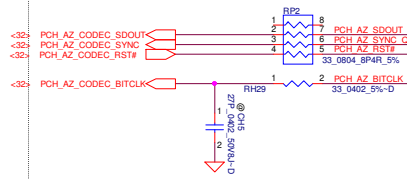
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

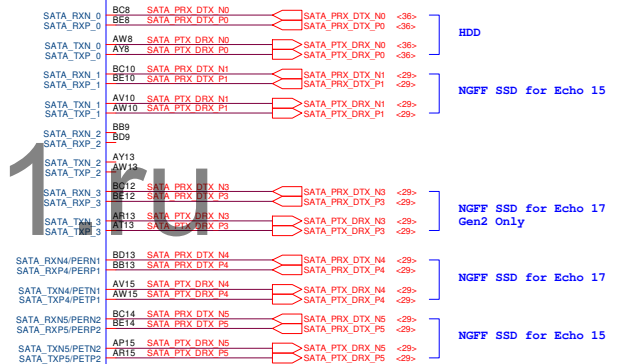
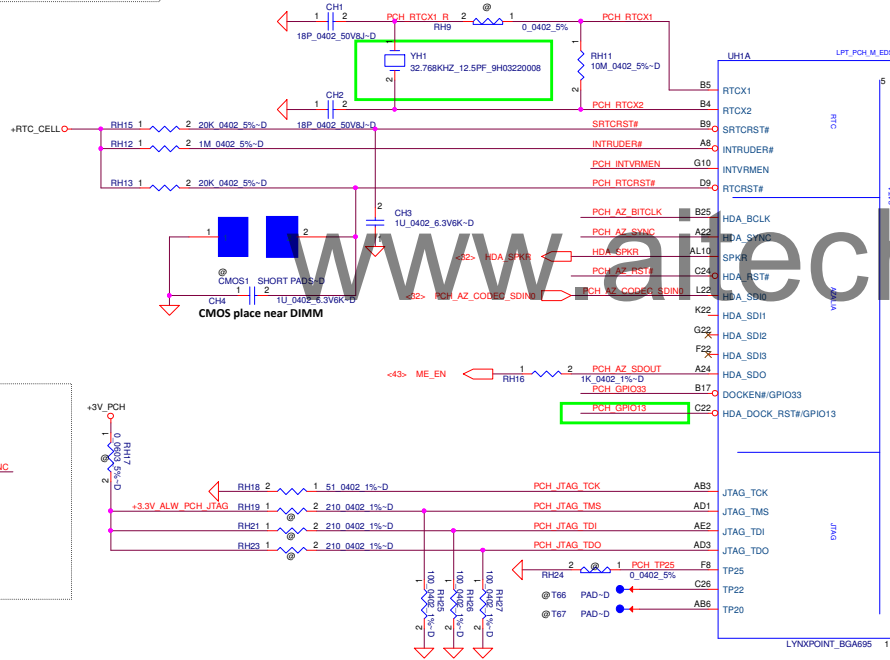
HDA_SYNC Isolation Circuit



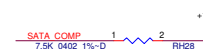
HDA for Codec and MDC



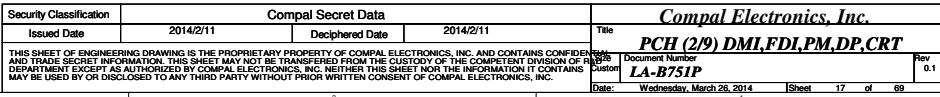
YH1 Change to SJ1000LD00 (ESR=50Kohm)

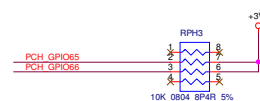
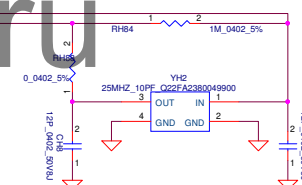
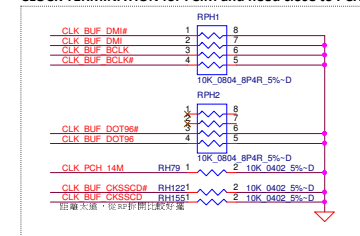
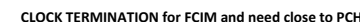



SATA Impedance Compensation

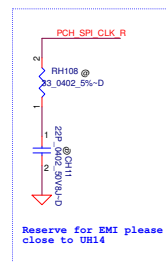
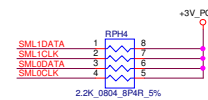
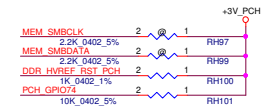
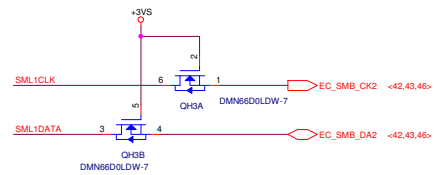


CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

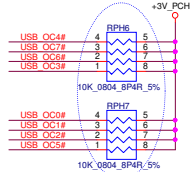
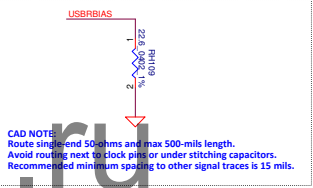




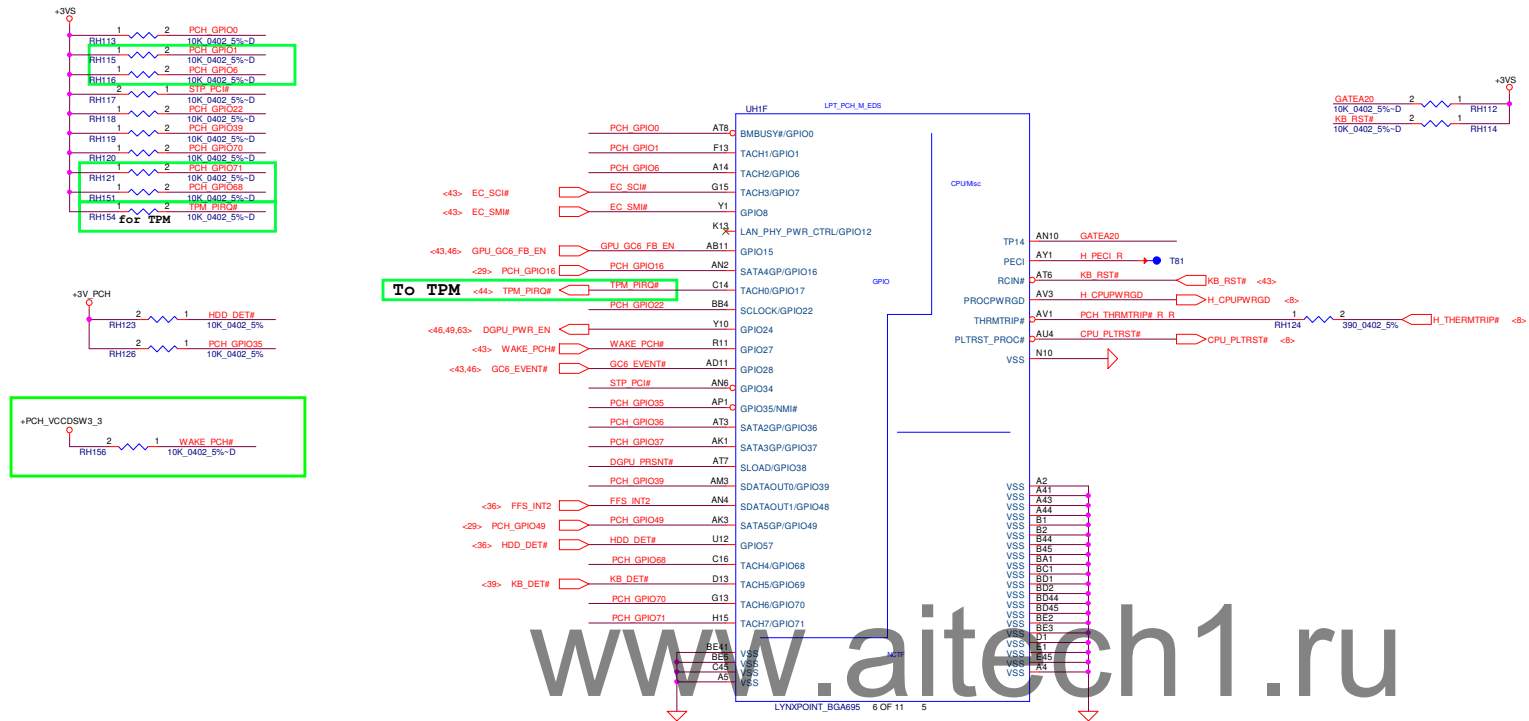
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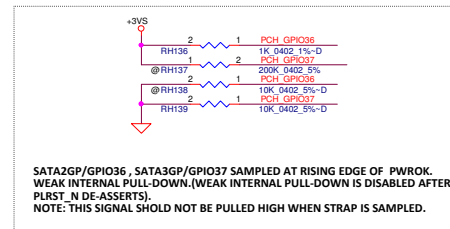
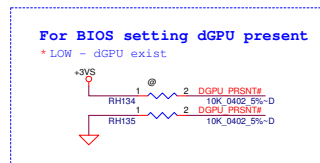
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			Document Number			
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			Customer: Wednesday, March 26, 2014			
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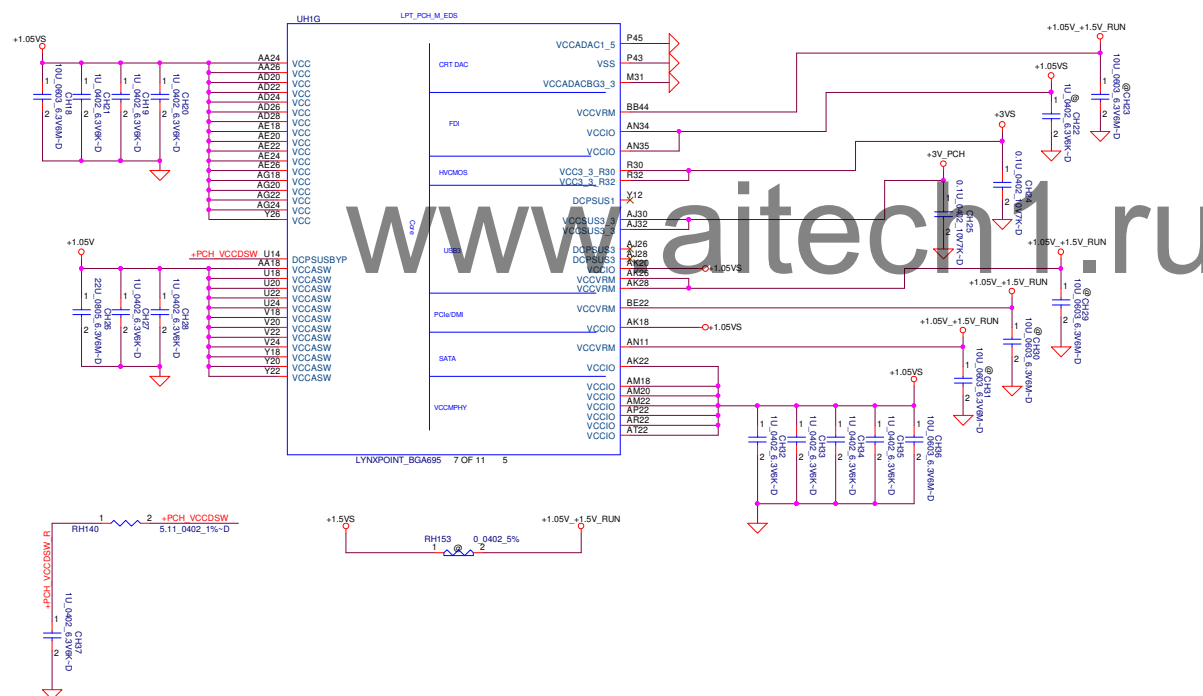


Config	GPIO16,49
USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

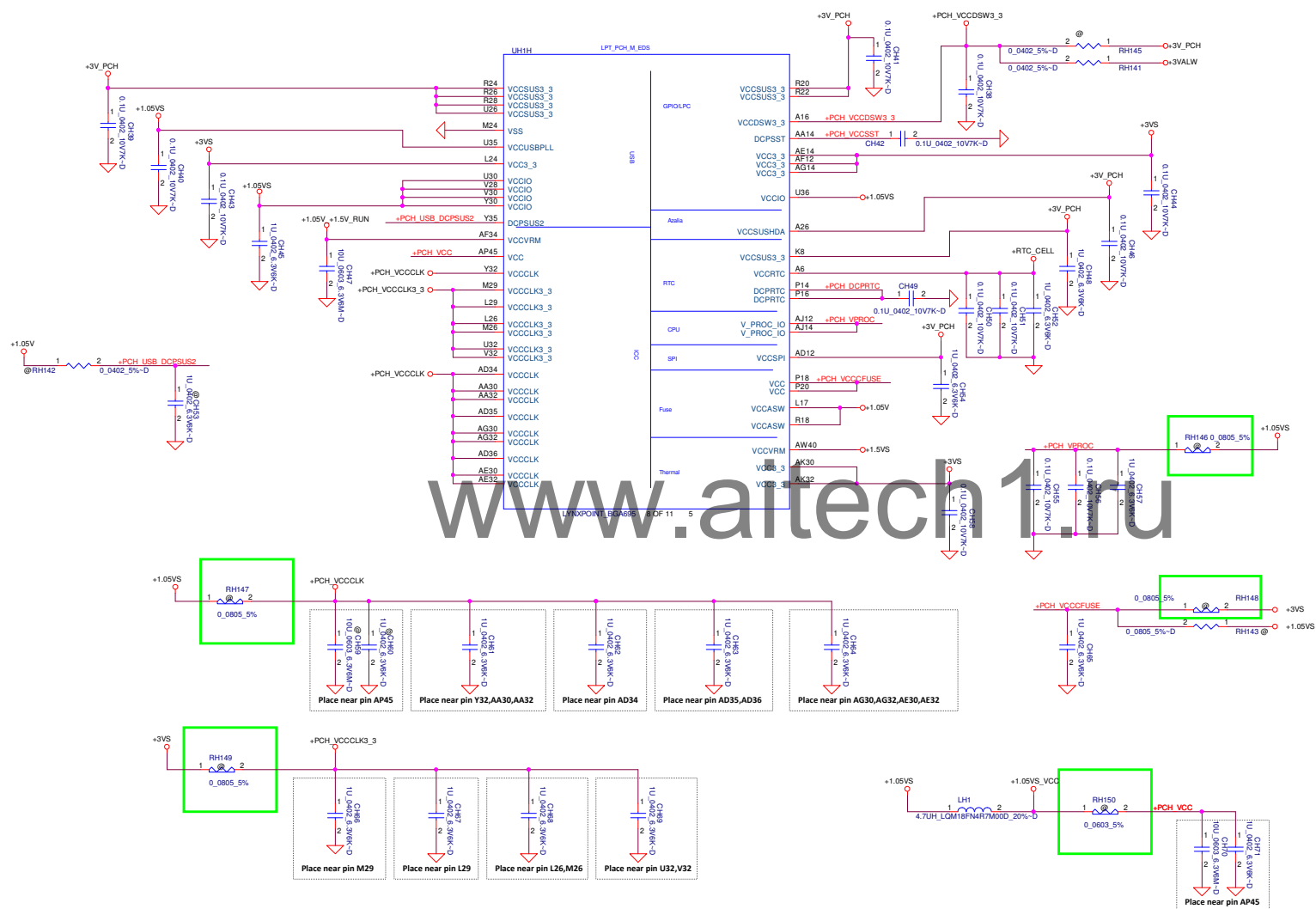


Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals					
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3				
				(00)	(00)							(00)	(00)								
				USB3 3	USB3 4							PCIE 1	PCIE 2								
				(01)	(01)							(01)	(01)								

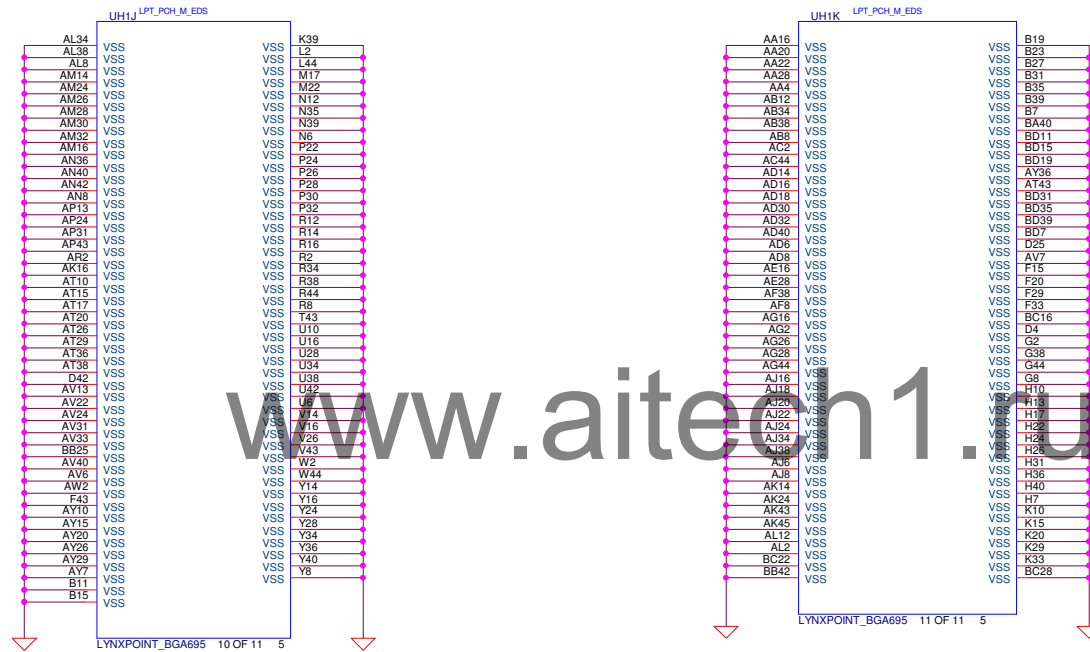
Same with 534345_PCH_LPT_9



PCH Power Rail Table

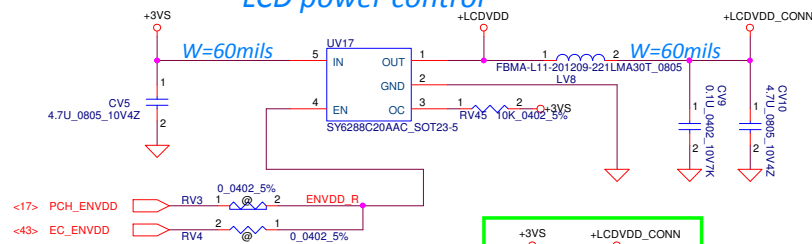


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Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title PCH (8/9) Power	
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				Rev. Revision 0.1	
Date:				Wednesday, March 26, 2014	Sheet 23 of 69

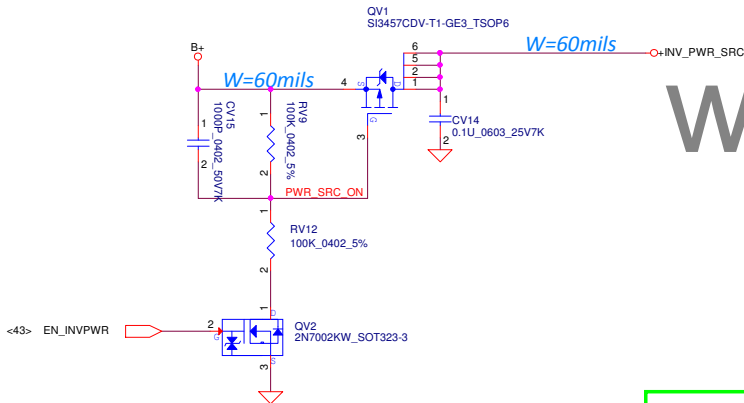


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				LA-B751P	0.1
				Date: Wednesday, March 26, 2014	Sheet 24 of 69

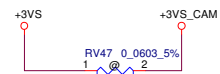
LCD power control



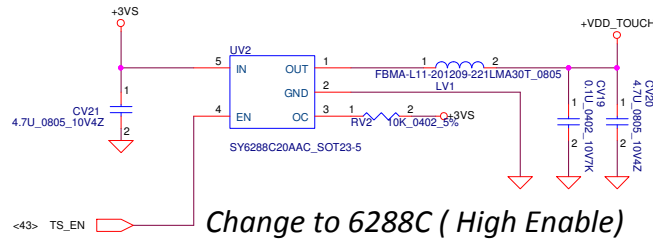
LCD backlight power control



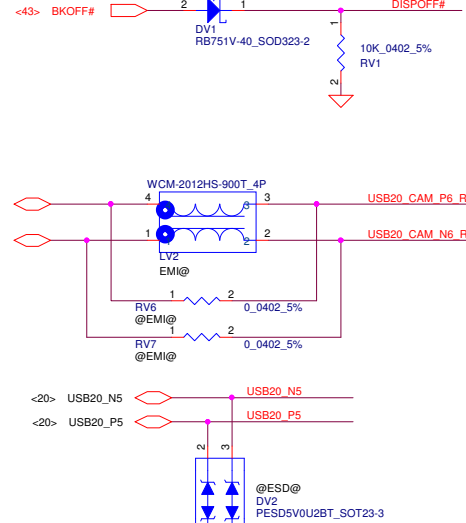
Webcam power control



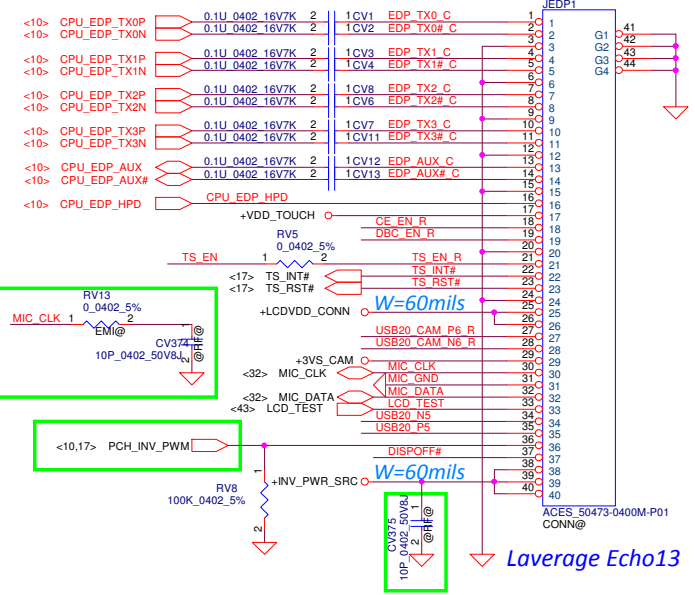
Touch screen panel power control



Change to 6288C (High Enable)



eDP connector

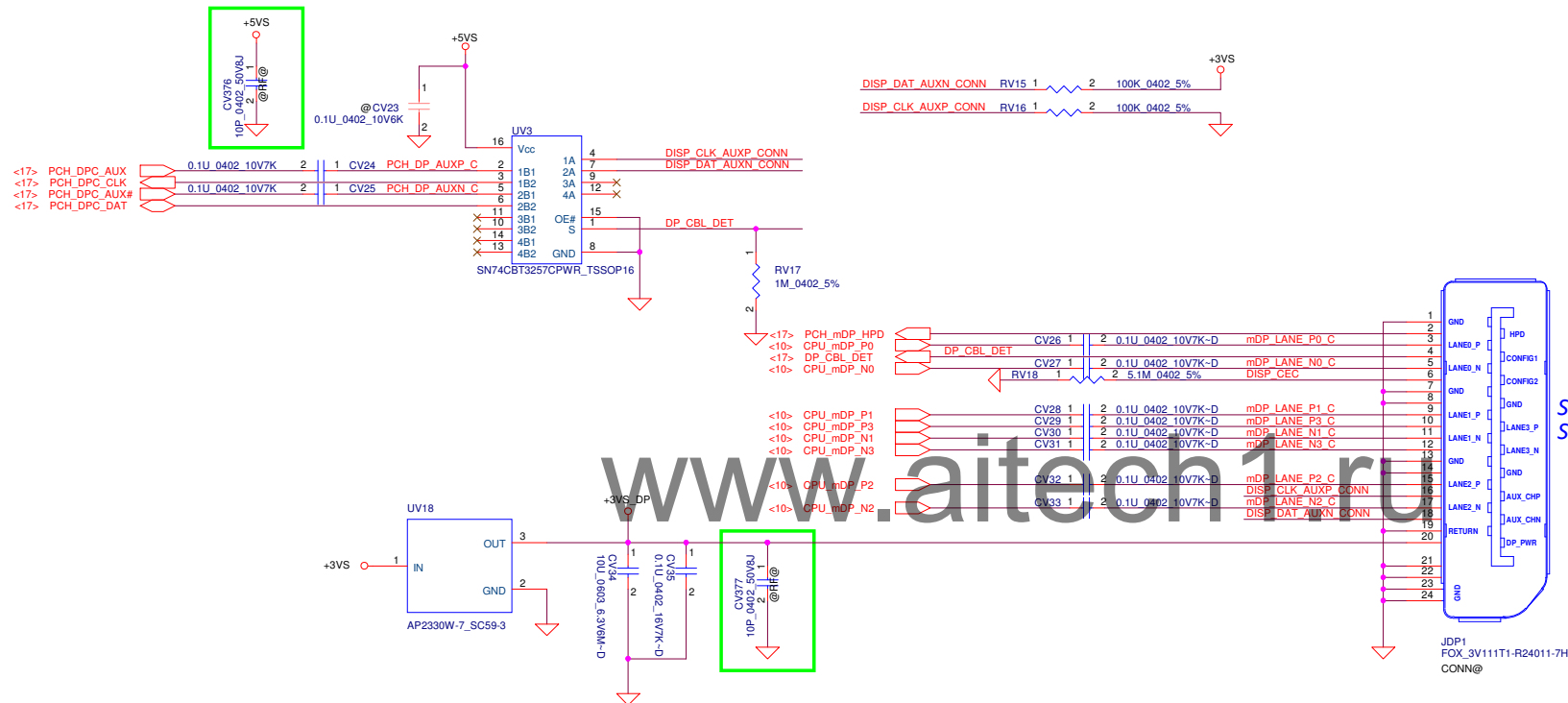


Lverage Echo13

Place close to JEDP

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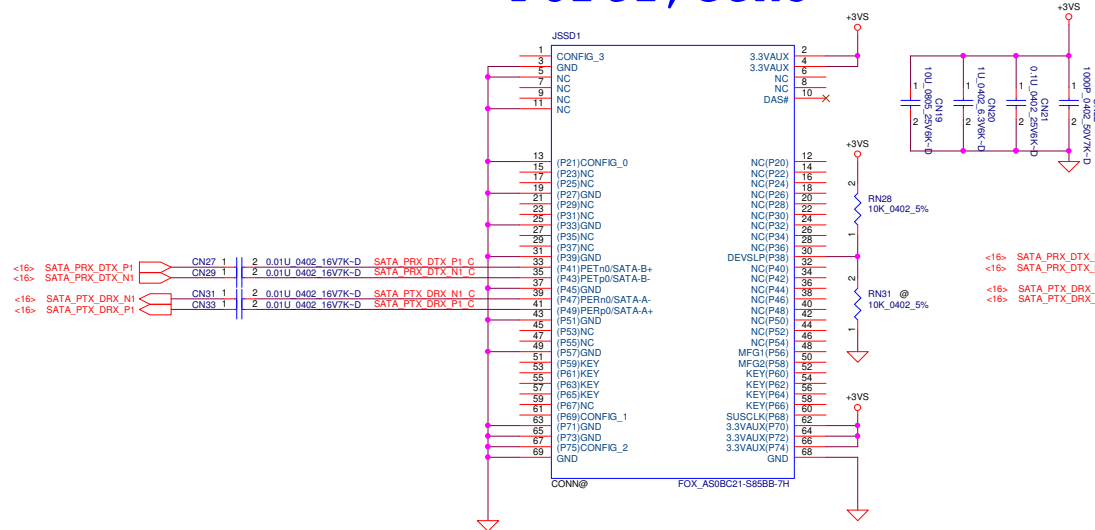
Security Classification	Compal Secret Data		Title	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Rev
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Compal Electronics, Inc.				Rev
LCD Conn/Cam, Touch				0.1
LA-B75IP				0.1
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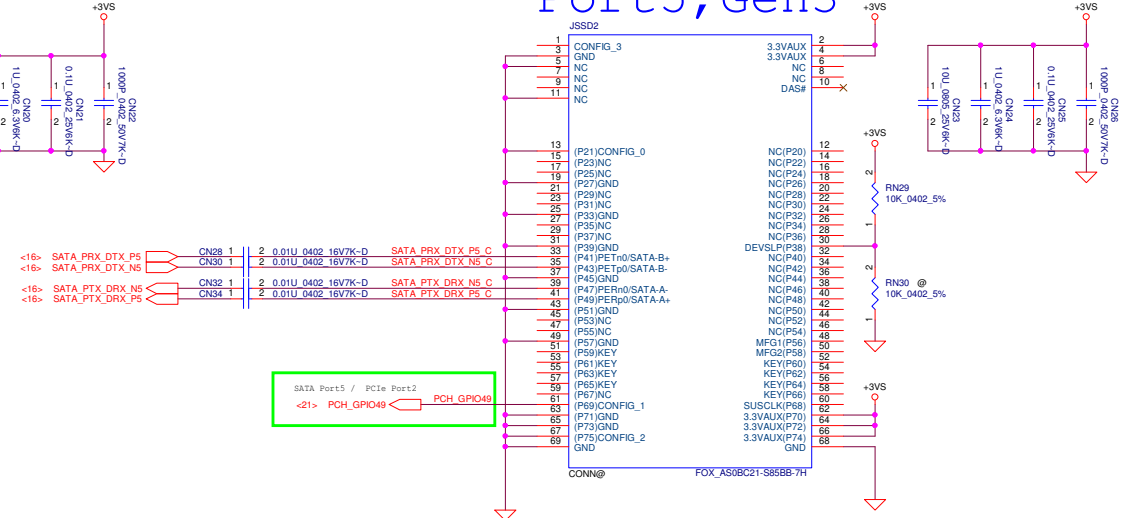
Same with ECHO13.
Symbol check OK. 2/25

Security Classification	Compal Secret Data			Title	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	3D Camera	
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				LA-B751P	0.1
				Date: Wednesday, March 26, 2014	Sheet 26 of 69

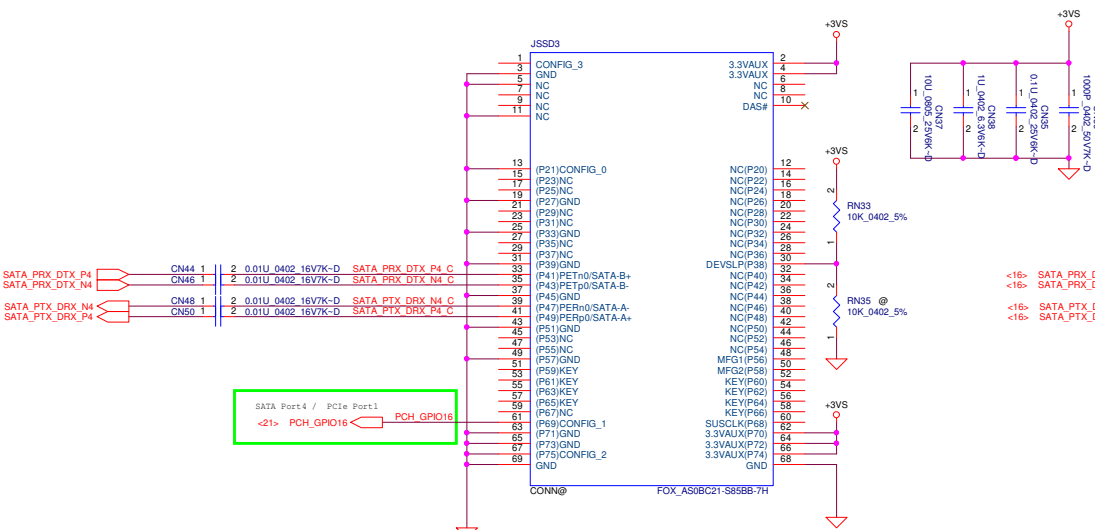
Port1, Gen3



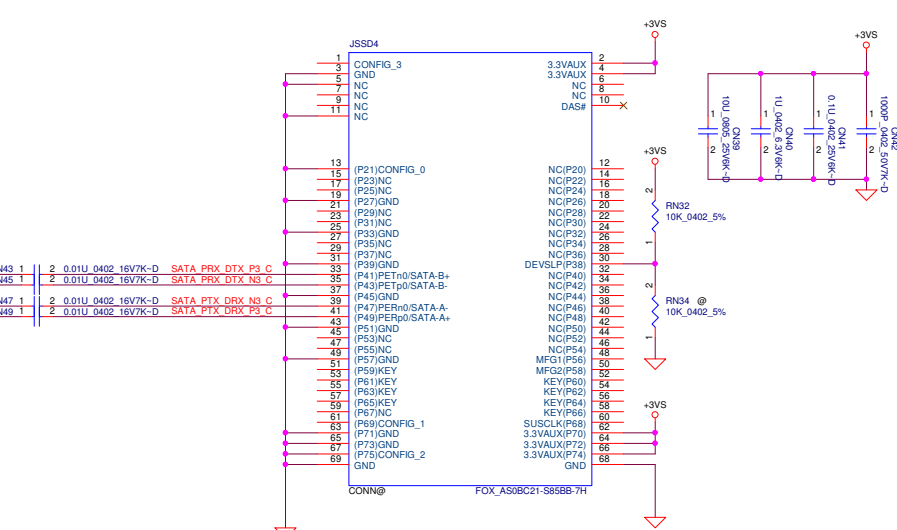
Port5, Gen3



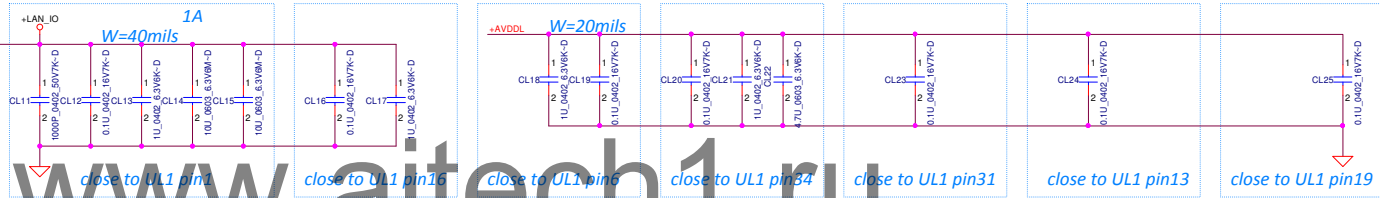
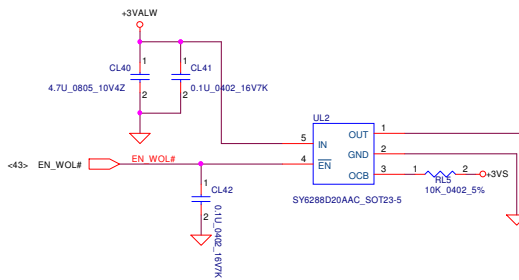
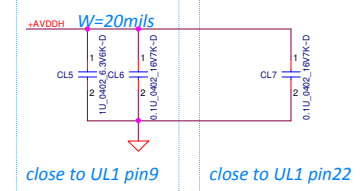
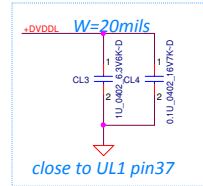
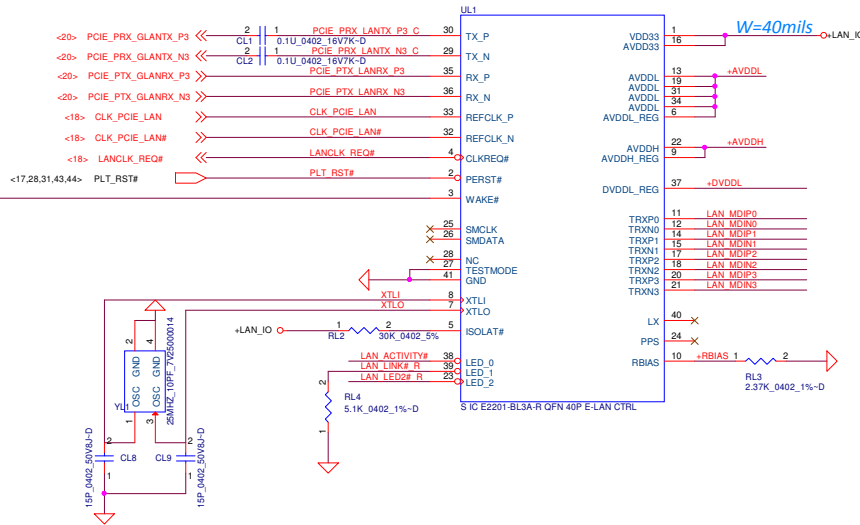
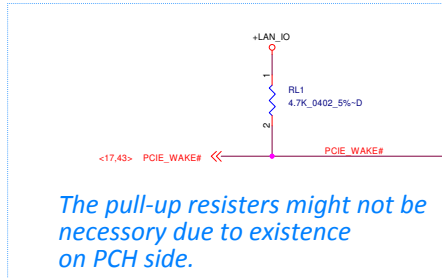
Port4, Gen3



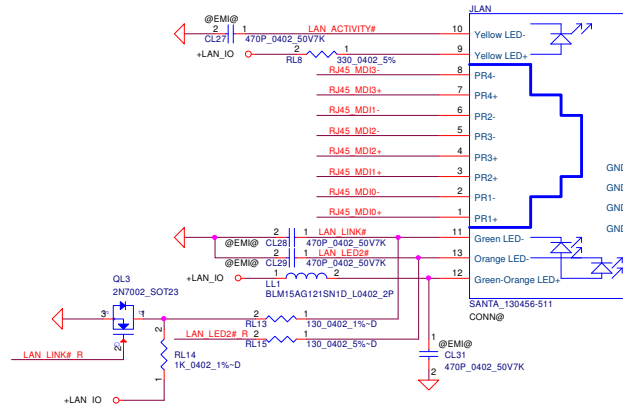
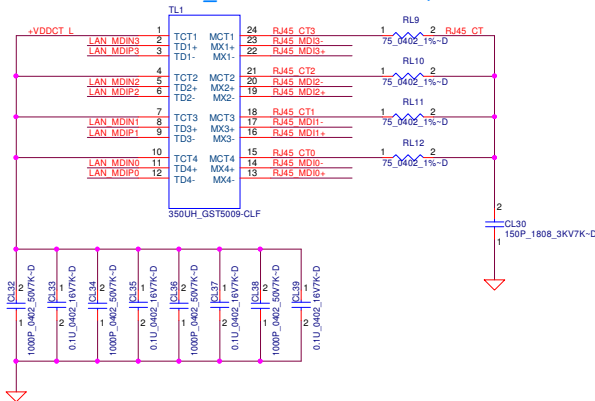
Port3, Gen2



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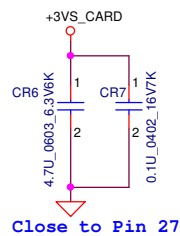


TIMAG: S X'FORM_IH-160 LAN,SP050006F00
BOTH HAND: S X'FORM_GST5009-D LF LAN,SP050006B00

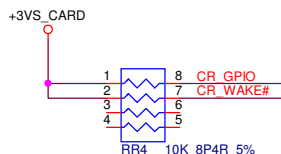


Same with ECHO13.
Symbol check OK. 2/25

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				Rev	0.1
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				Sheet	30 of 60

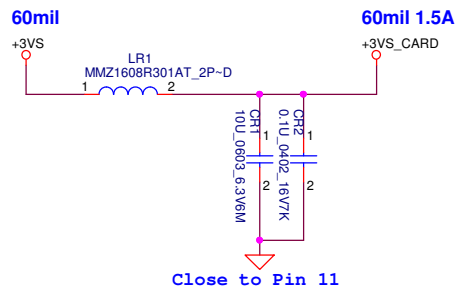


<20> PCIE_PTX_CARDRX_P5 >> PCIE_PTX_CARDRX_P5
 <20> PCIE_PTX_CARDRX_N5 >> PCIE_PTX_CARDRX_N5
 <20> PCIE_PRX_CARDTV_P5 << PCIE_PRX_CARDTV_P5
 <20> PCIE_PRX_CARDTV_N5 << PCIE_PRX_CARDTV_N5



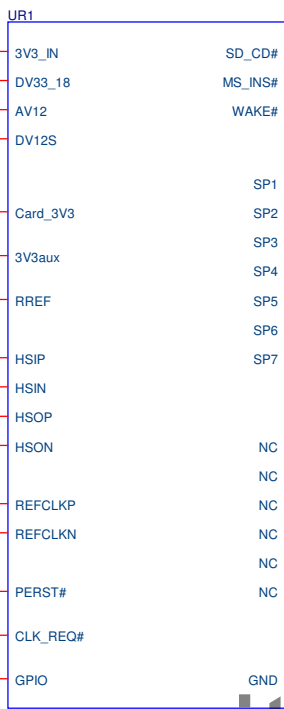
<18> CLK_PCIE_CD >> CLK_PCIE_CD
 <18> CLK_PCIE_CD# >> CLK_PCIE_CD#

<17,28,30,43,44> PLT_RST# >> PLT_RST#
 <18> CDCLK_REQ# << CDCLK_REQ#



Close to Pin 11

pin28:
 If GPIO NO use for LED function and
 GPIO must pull high



RTS5227-GR-QFN32_4X4

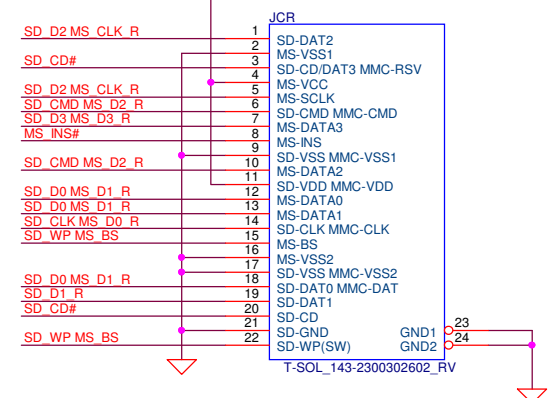
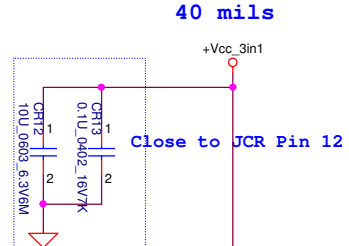
Internal Pull status

	NO Card	SD Insert	MS Insert
15_SP1	PD80	SD_D1_PU80	PD80
16_SP2	PD80	SD_D0_PU80	MS_D1_PD80
17_SP3	PD80	SD_CLK_PD80	MS_D0_PD80
19_SP4	PD80	SD_CMD_PU80	MS_D2_PD80
20_SP5	PD80	SD_D3_PU80	MS_D3_PD80
21_SP6	PD80	SD_D2_PU80	MS_CLK_PD80
29_SP7	PD200	SD_WP_PD200	MS_BS_PD200
30_SD_CD#	PU200	PU200	PU200
31_MS_CD#	PU200	PU200	PU200

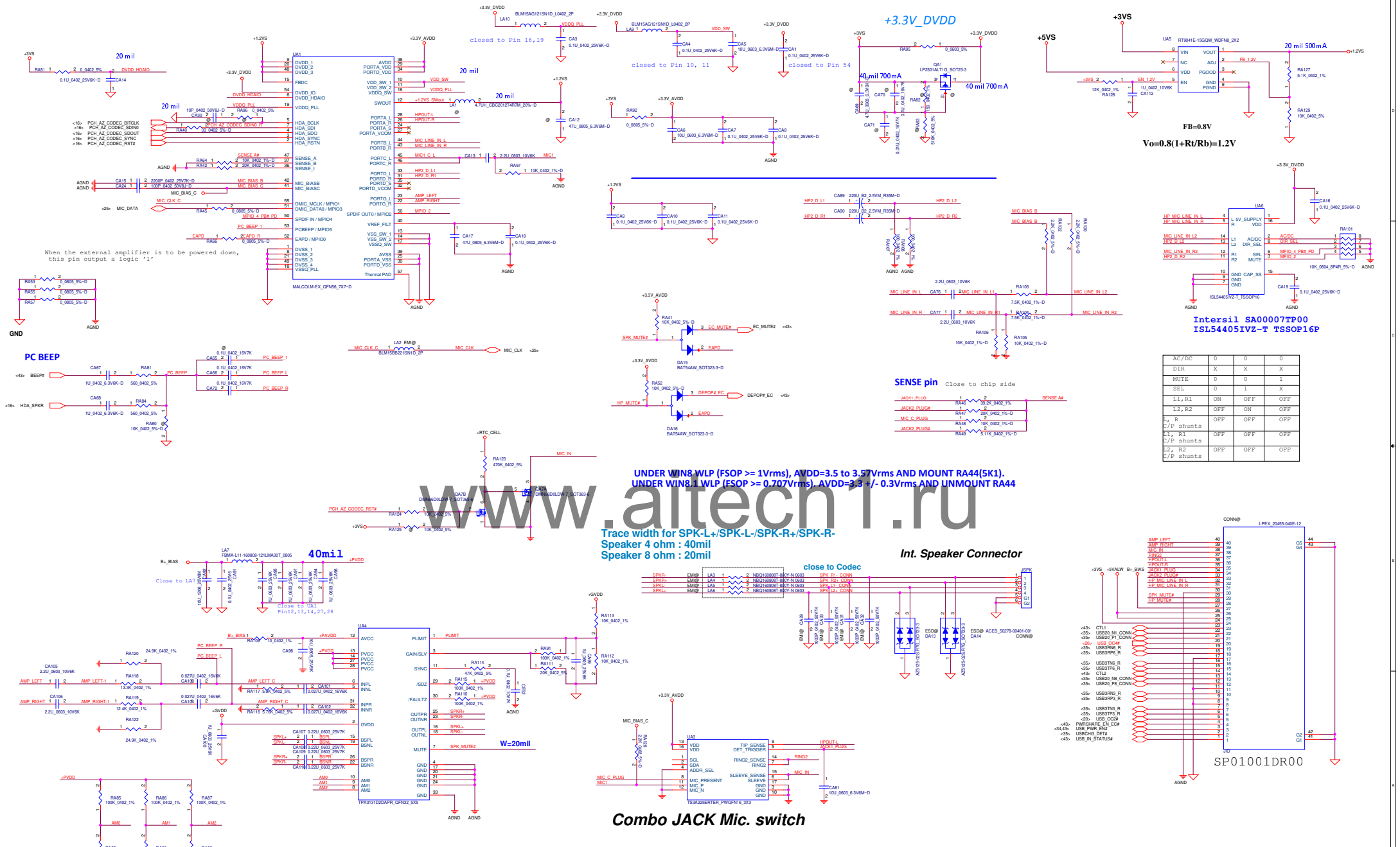
SD_CD# 30
 MS_INS# 31
 WAKE# 32

SP1 15
 SP2 16
 SP3 17
 SP4 19
 SP5 20
 SP6 21
 SP7 29

for project which need fine tune SD signal can change to R



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UNDER WIN8 WLP (FSOP >= 1Vrms), AVDD=3.5 to 3.57Vrms AND MOUNT RA44(5K1).
UNDER WIN8.1 WLP (FSOP >= 0.707Vrms), AVDD=3.3 +/- 0.3Vrms AND UNMOUNT RA44

Trace width for SPK-L+SPK-L+SPK-R+SPK-R
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

Int. Speaker Connector

Combo JACK Mic. switch

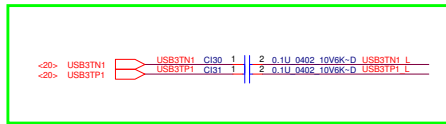
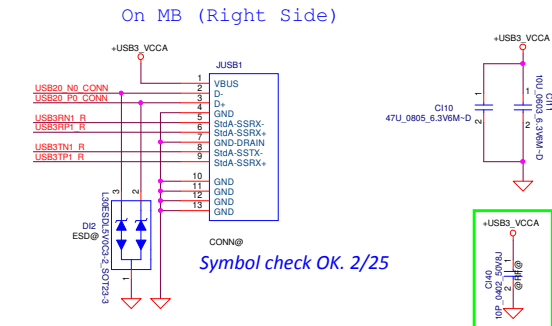
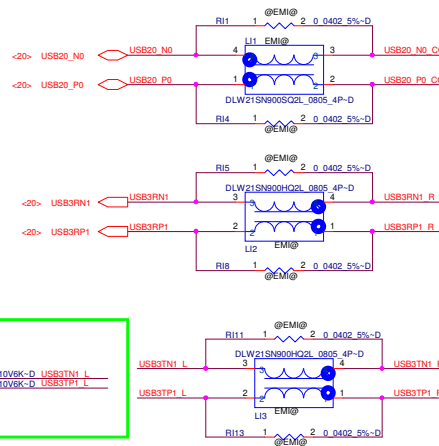
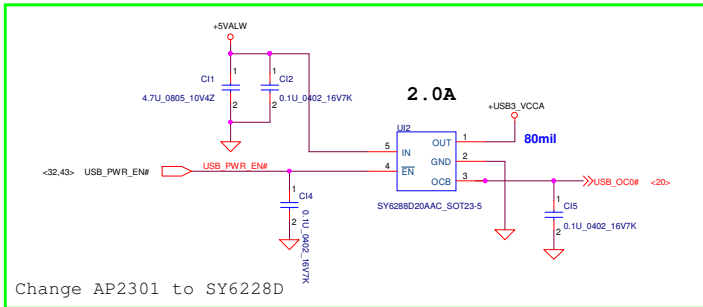
AC/DC	0	0	0
D1K	X	X	X
MUTE	0	0	1
SEL	0	1	X
L1, R1	ON	ON	OFF
L2, R2	OFF	ON	OFF
C/P shunts	OFF	OFF	OFF
L1, R1	OFF	OFF	OFF
L2, R2	OFF	OFF	OFF
C/P shunts	OFF	OFF	OFF

SP01001DR00

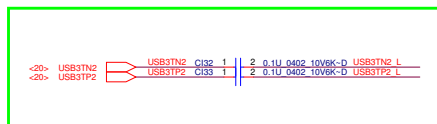
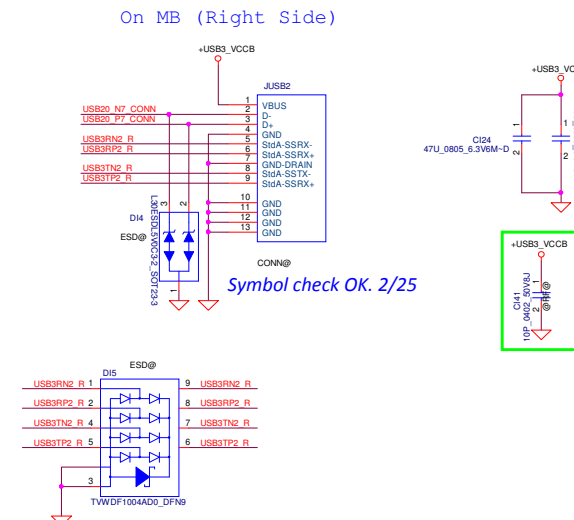
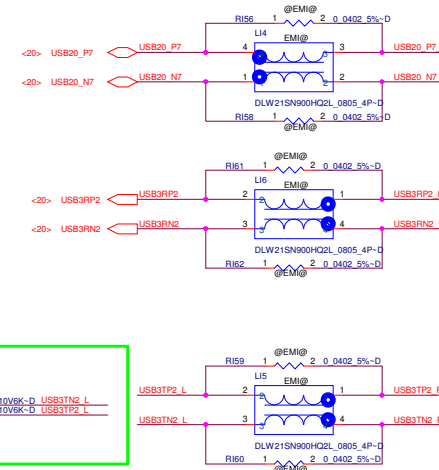
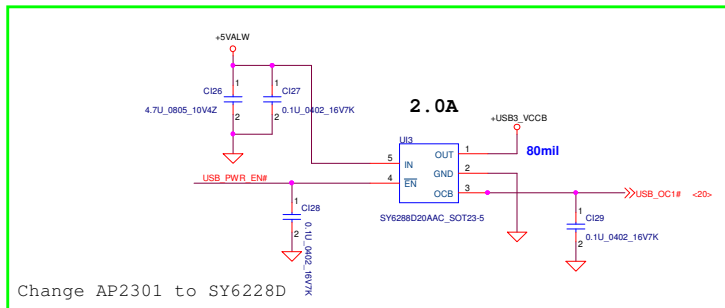
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2011/06/02		Declassified Date		2012/06/02	
Issued Date				Codec Malcom-EX	
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LA-8381P				1.0	
Date				Rev	
2011/06/02				2012/06/02	

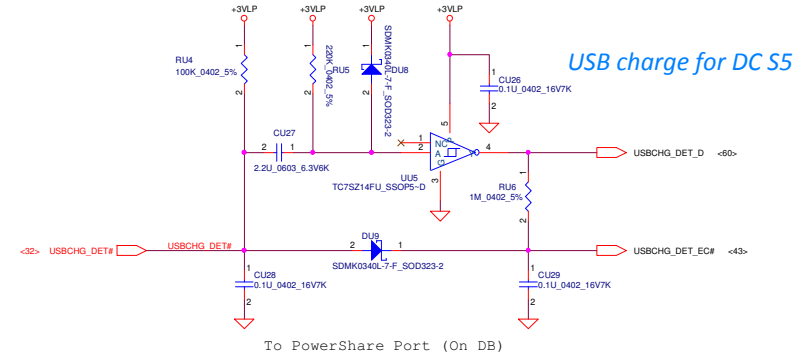
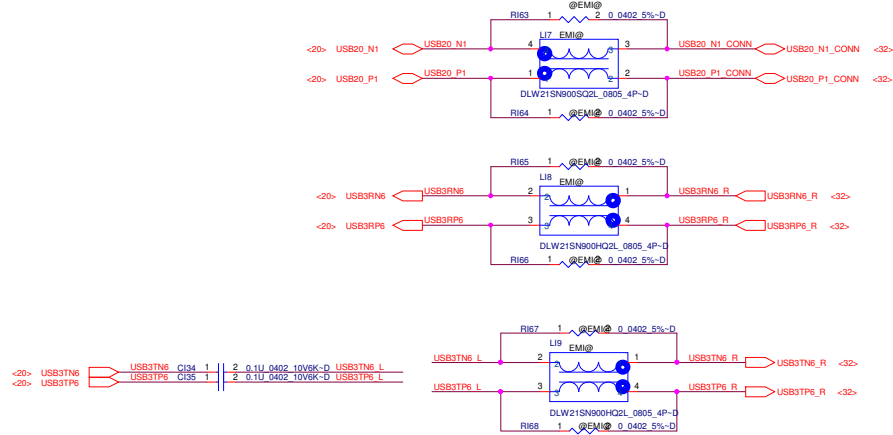
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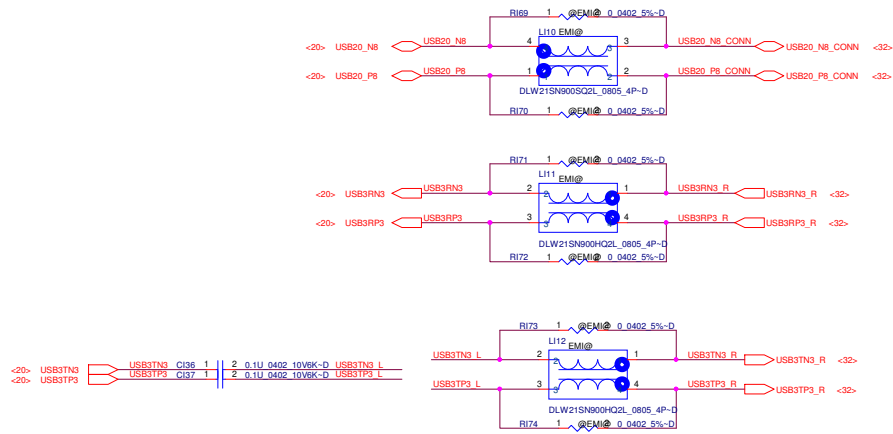


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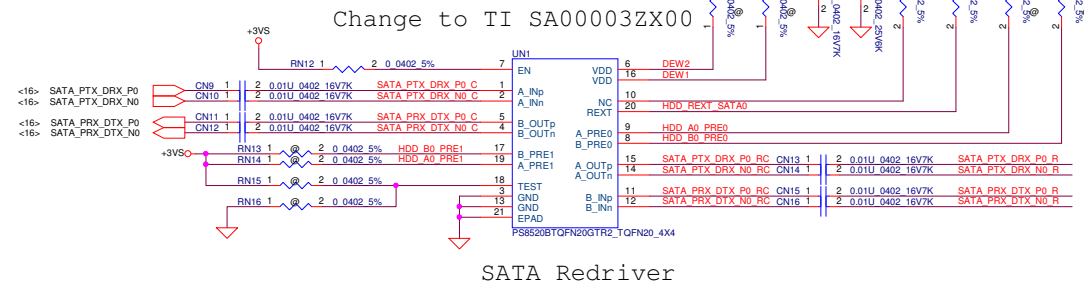




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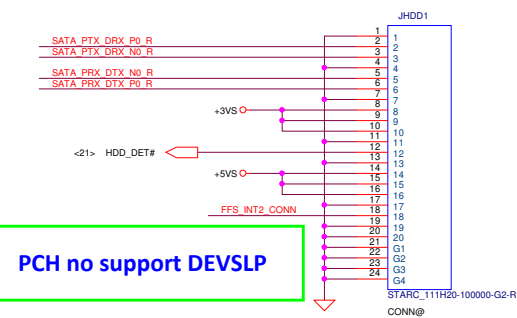
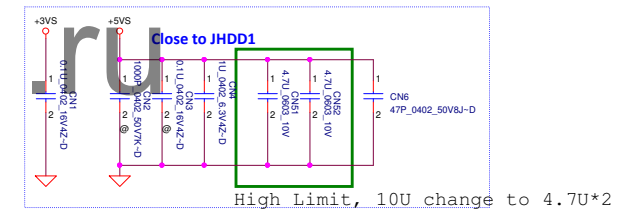
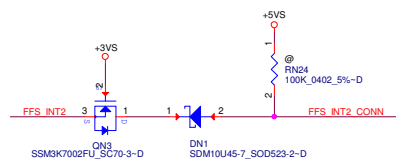
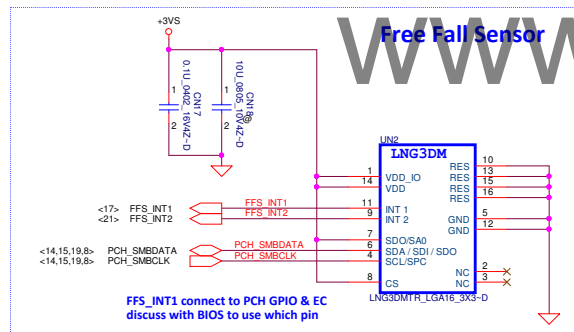
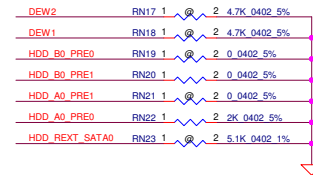


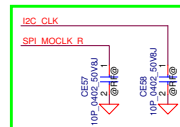
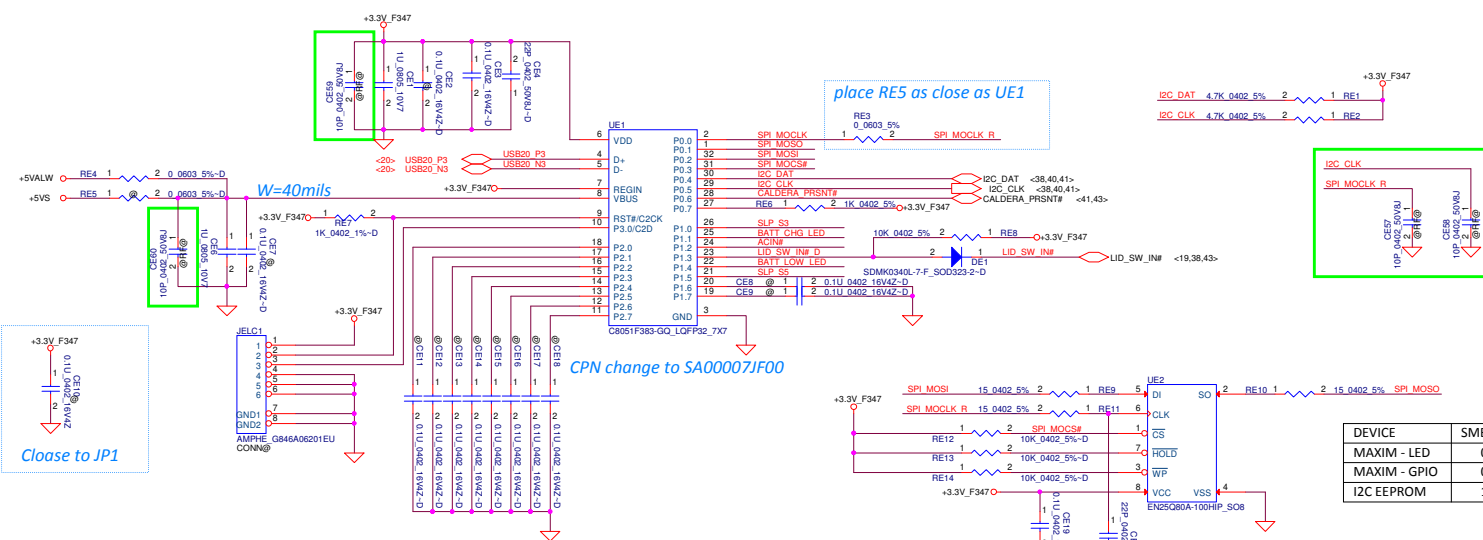
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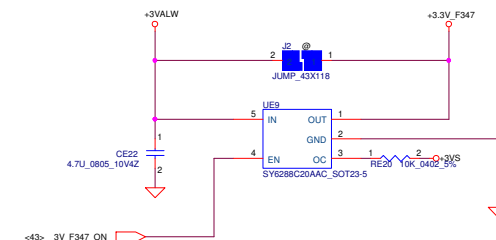
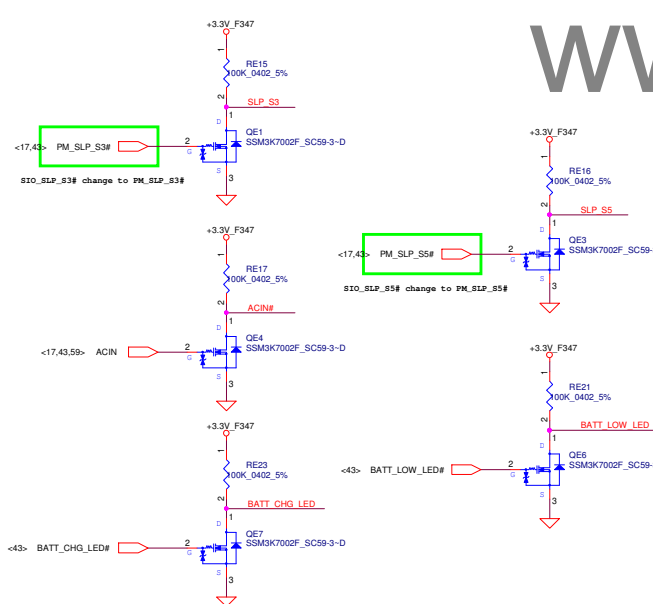
Pin 20:
PARADE PS8250B
Depop RS26
PERICOM PI3EQX6741ST
Pop RS26
ASMEDIA ASM1466
Pop RS26

Pin 9:
PARADE PS8250B
Depop RS24
PERICOM PI3EQX6741ST
Depop RS24
ASMEDIA ASM1466
Pop RS24 to pull down





DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b



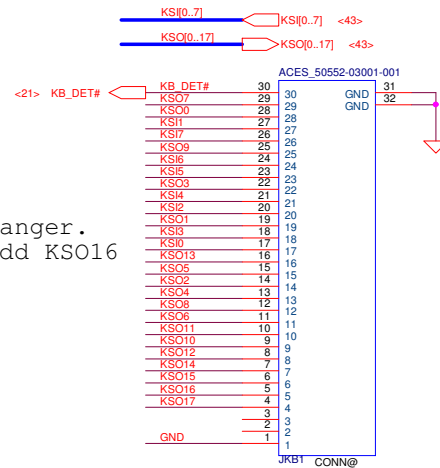
+3V_F347 behavior

	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BATT only	ON	ON	OFF	OFF

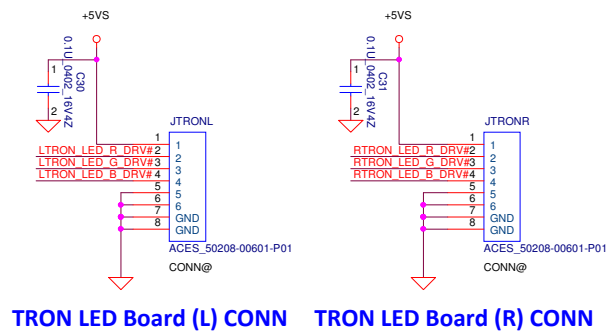
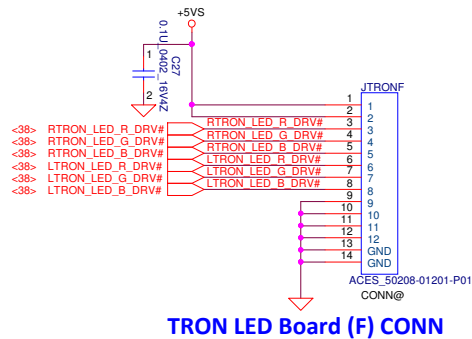
AC mode battery full in S5: turn off ELC controller

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INT_KBD Conn.

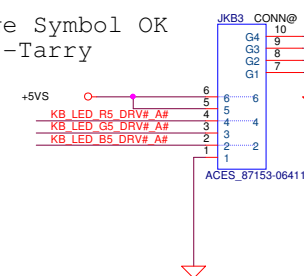


Net follow Ranger.
Only Pin26 add KSIO16

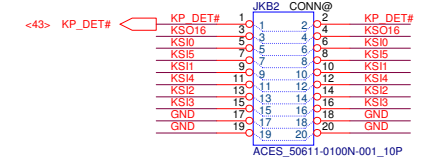


Hot Key Conn. PWM

Change Symbol OK
2/18 -Tarry



Hot Key Conn. Key Pad



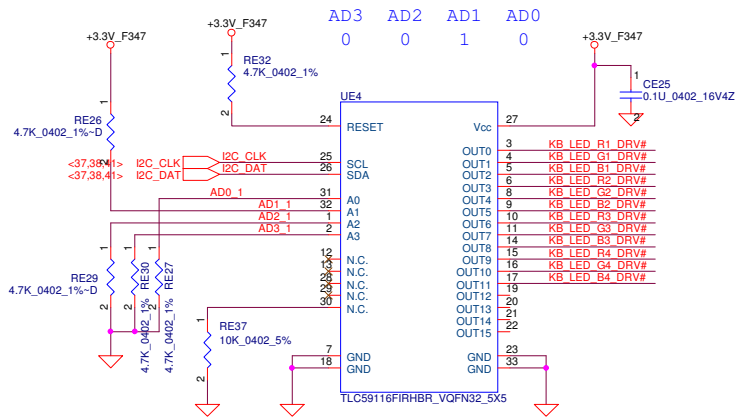
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.			
Title	KB/HotKey conn		
Size	Document Number	Rev	
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Date:	Wednesday, March 26, 2014	Sheet	39 of 69

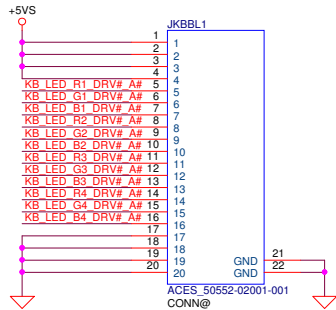
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K/B Backlight



Check Pin define



KB BL LED

Symbol OK (Leverage Echo13)
2/18 -Tarry



DELL CONFIDENTIAL/PROPRIETARY

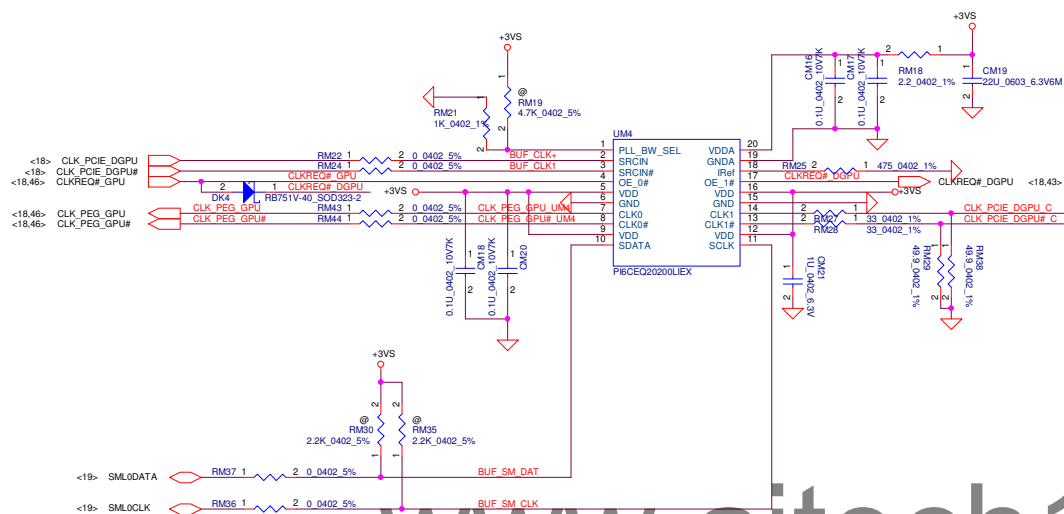


Compal Electronics, Inc.			
Title			
ELC(3)			
Size	Document Number	Rev	
	LA-B751P	0.1	
Date:	Wednesday, March 26, 2014	Sheet	40 of 69

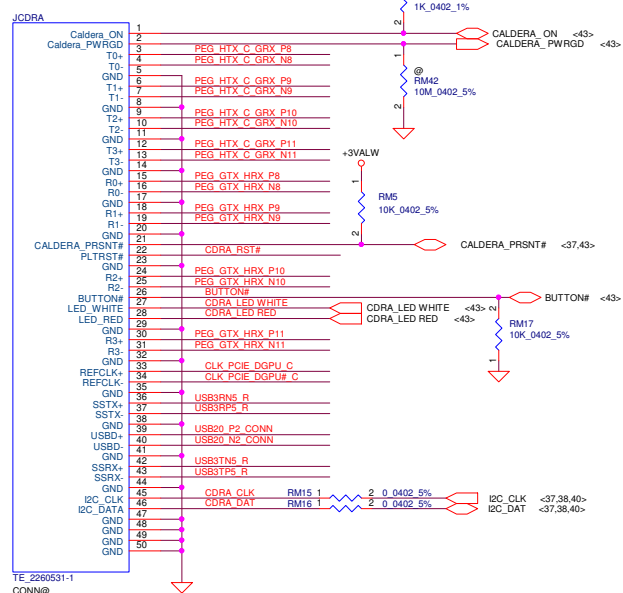
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EC控制/PIN
PCI_SMCLK
PCI_SMDAT
USB_PWR_EN#
DOCKING_LED ON#
DOCKING_LED OFF#
DOCK_PSID
DOCK_ACIN
DOCK_EN
PRSNT# R

PCIE CLK BUFFER

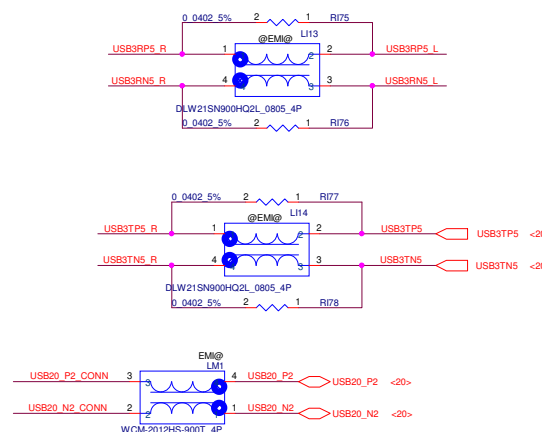


Caldera connector

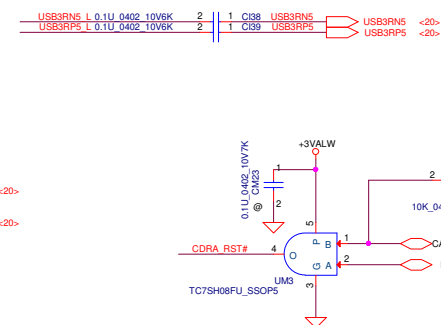


Symbol OK (Leverage Echo13)
2/18 -Tarry

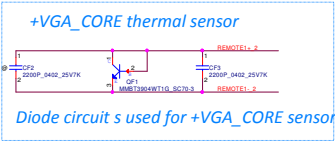
Diagram showing four input lines (two blue, two red) connected to a single output line labeled "Caldera". The inputs are labeled: PEG_HTX_C_GRX_P[8..11] <7>, PEG_HTX_C_GRX_N[8..11] <7>, PEG_GTX_HRX_P[8..11] <7>, and PEG_GTX_HRX_N[8..11] <7>.



Follow Echo 13 design.

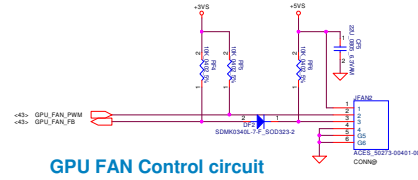
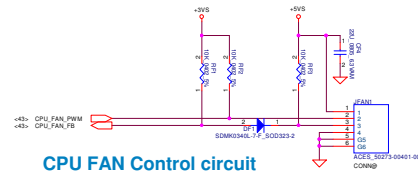
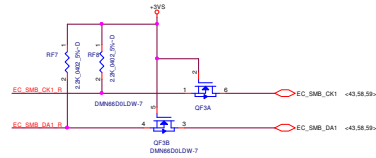
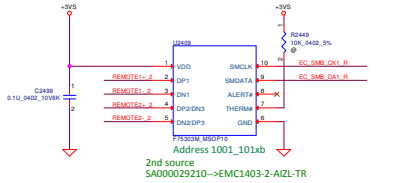
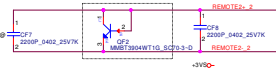


Security Classification		Compal Secret Data		<div> <div>Compal Electronics, Inc.</div> <div> <div>USB3.0</div> <div>Document Number</div> <div>LA-B751P</div> </div> </div>	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	Rev 0.1
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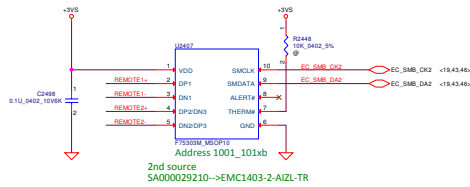


SKIN

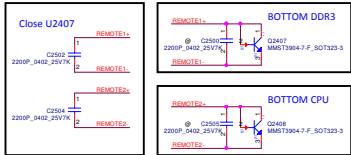
Diode circuit s used for skin temp sensor
(placed around DIMM).
Place C43 close to Q15as possible.



Fintek thermal sensor-> CPU core, DIMM

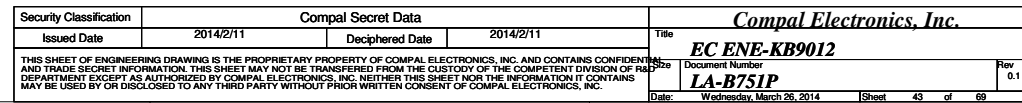


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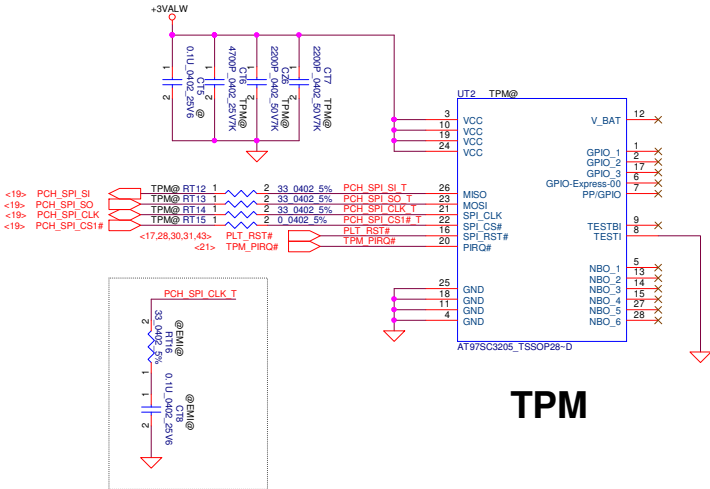


REMOTE1,2 (+/-):
Trace width/space:10/10 mil
Trace length:<8"

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Issued Date	2014/2/11	Discontinued Date	2014/2/11	Rev
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LA-B751P				Rev
Wednesday, March 26, 2014				Rev



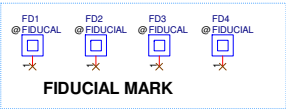
02/18 Add TPM Function (Follow ZAM60)



TPM

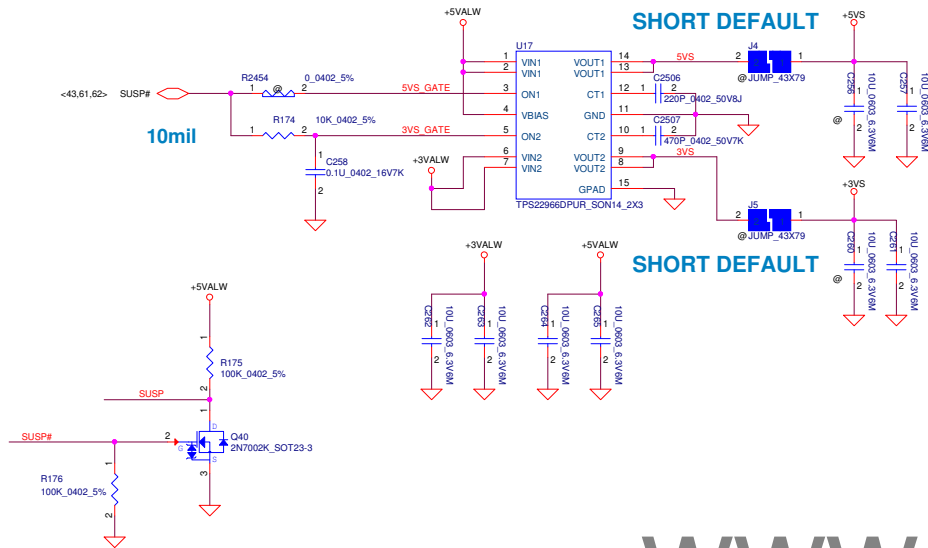
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Screw Hole



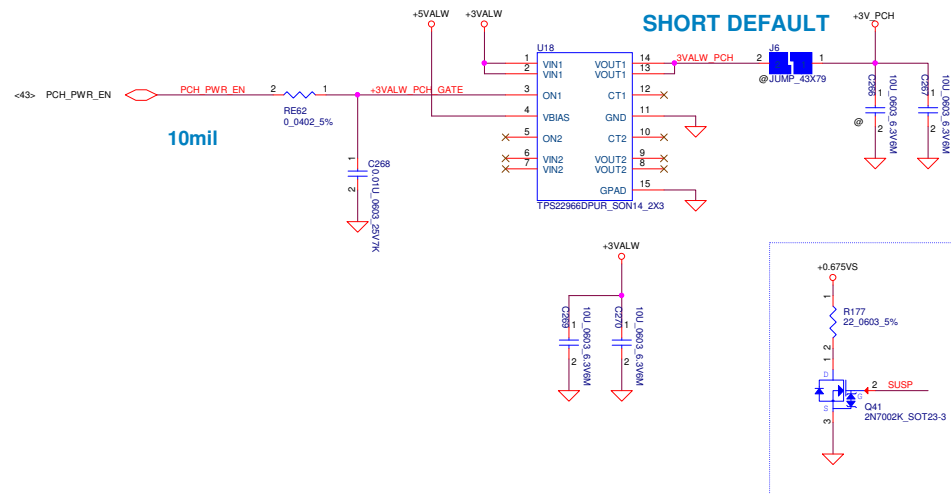
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	Screw Hole
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				Date	Wednesday, March 26, 2014
				Sheet	44 of 69
				Rev	0.1

+5VS and +3VS switch



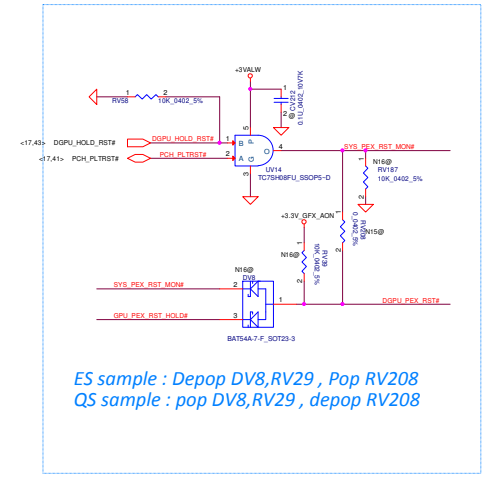
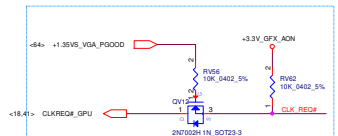
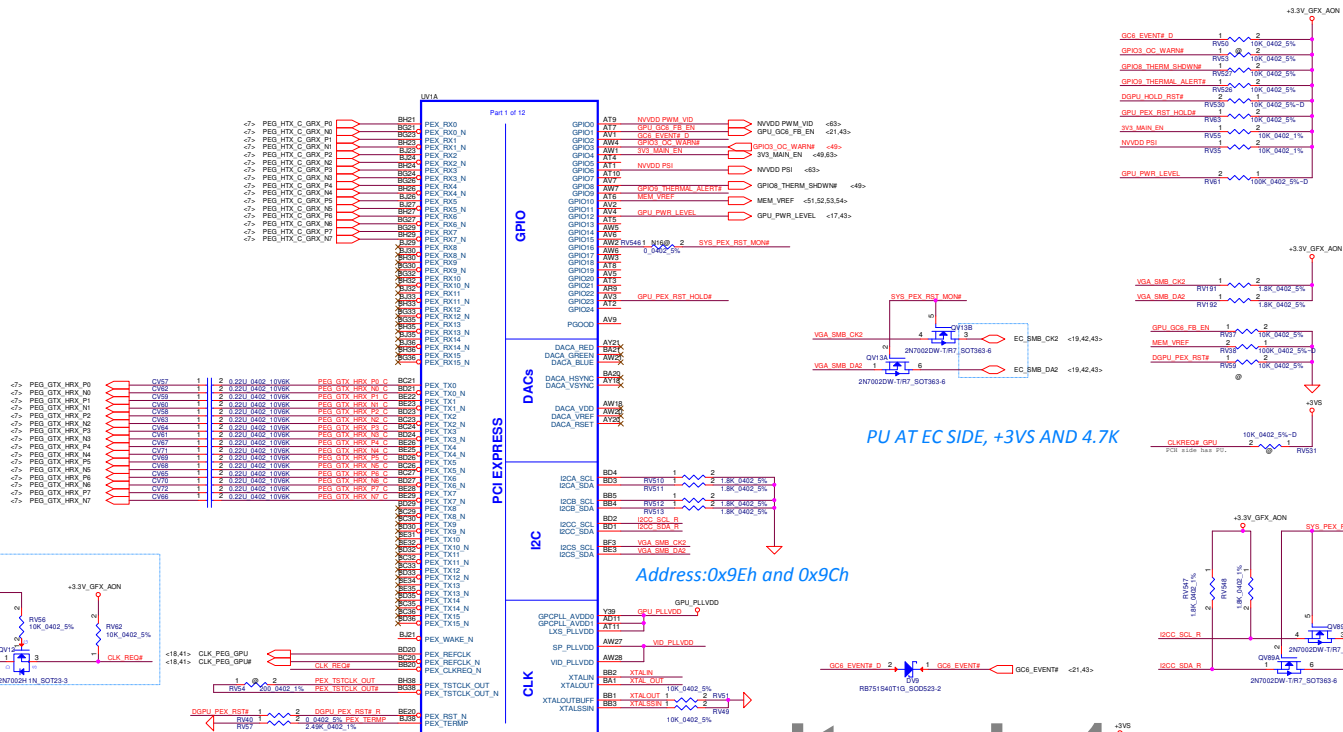
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+3VALW_PCH switch



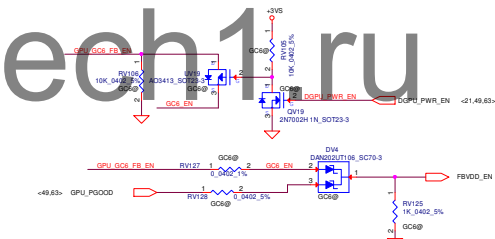
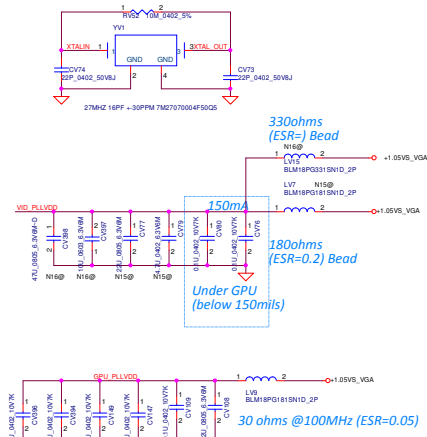
For Intel S3 Power Reduction

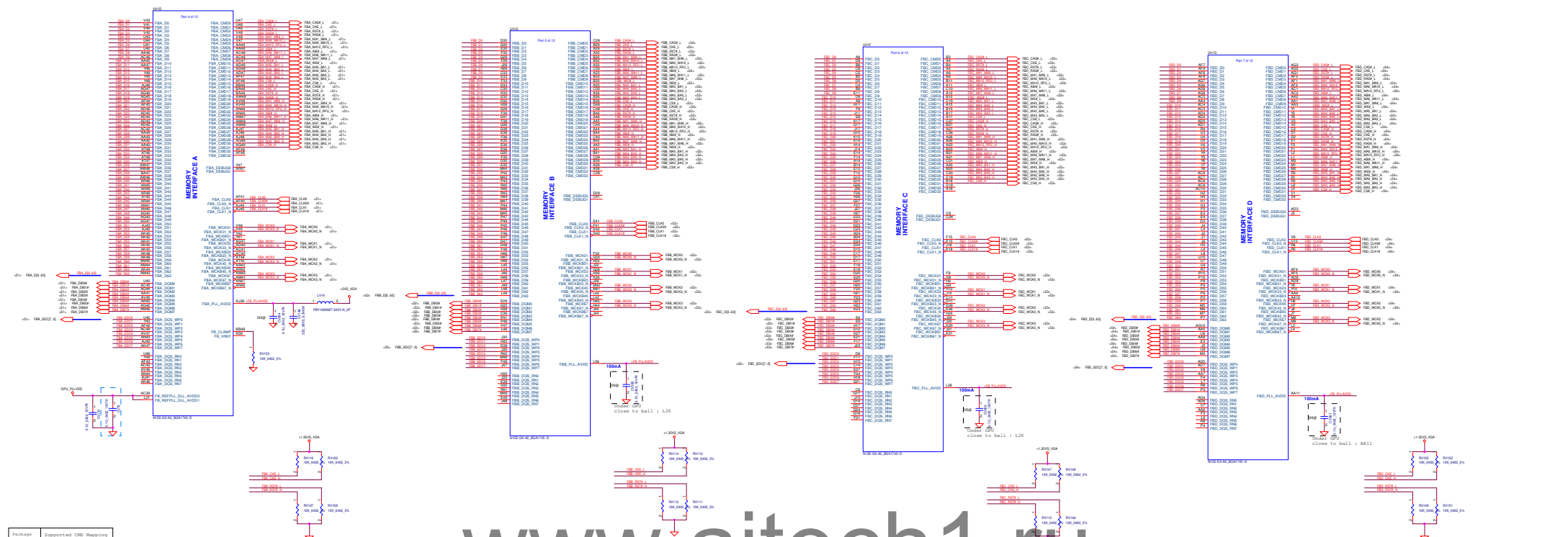
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title	DC/DC Interface
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				LA-B751P	0.1
Date: Wednesday, March 26, 2014				Sheet	45 of 69



ES sample : Depop DV8,RV29 , Pop RV208
 QS sample : pop DV8,RV29 , depop RV208

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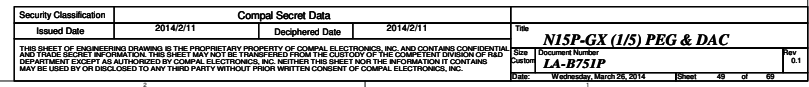
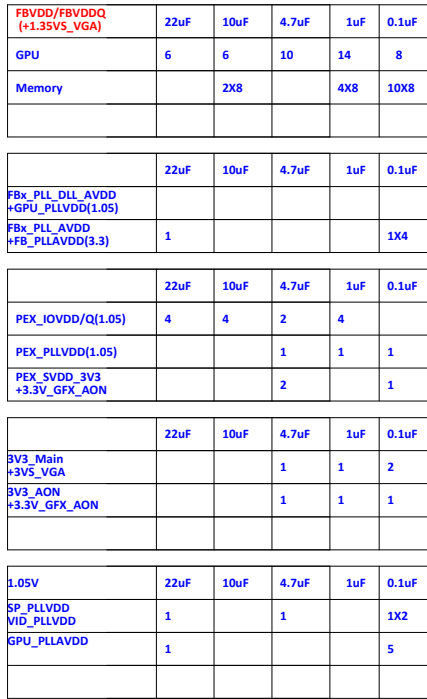


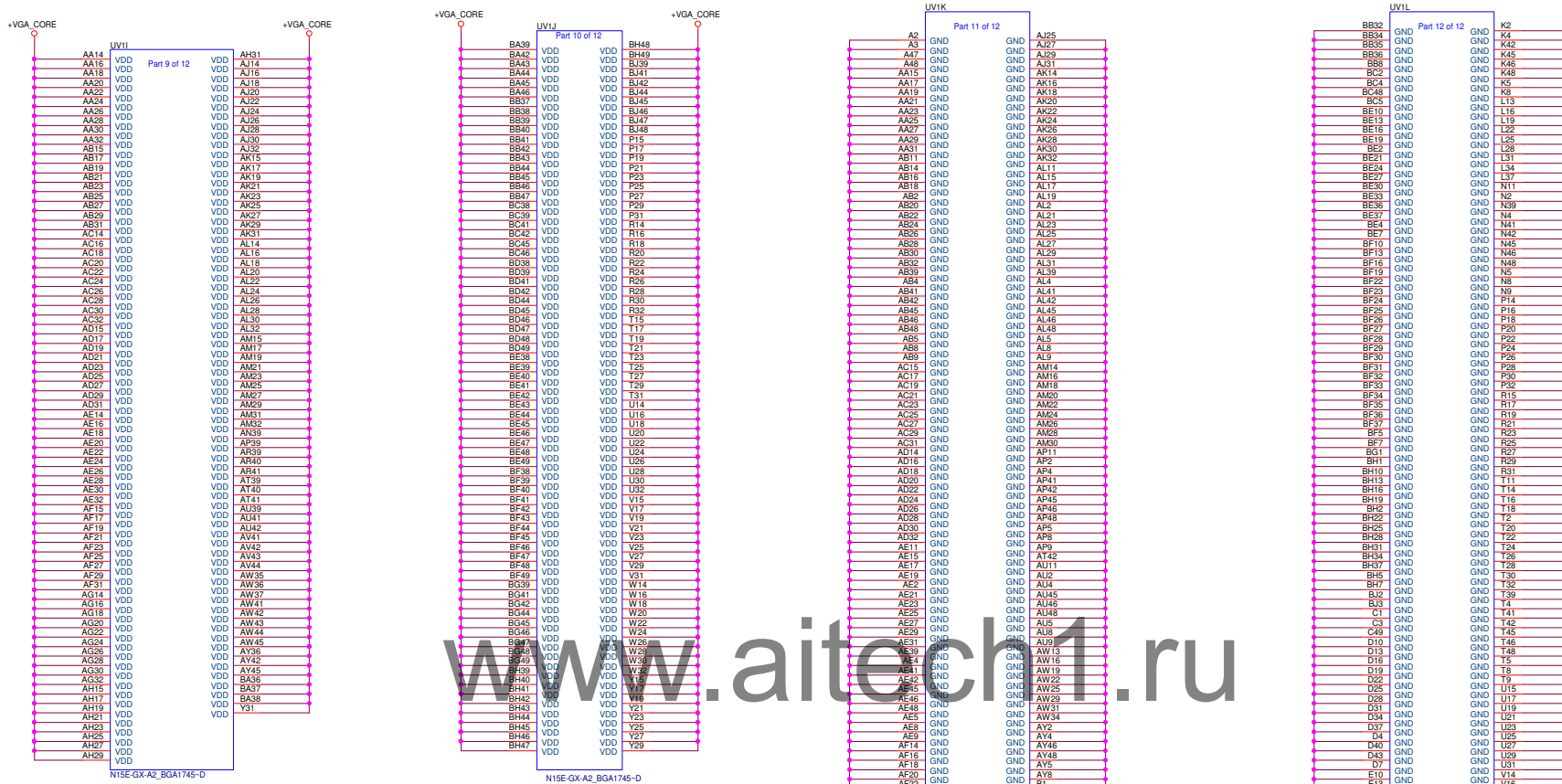
Package	Supported QMC Mapping
QMC1-44	
QMC1-12	Y
QMC1-206	Y

Node A Address	0...31	Node B Address	32...63
QMC1	QMC1_0	QMC1_32	QMC1_64
QMC2	QMC2_0	QMC2_32	QMC2_64
QMC3	QMC3_0	QMC3_32	QMC3_64
QMC4	QMC4_0	QMC4_32	QMC4_64
QMC5	QMC5_0	QMC5_32	QMC5_64
QMC6	QMC6_0	QMC6_32	QMC6_64
QMC7	QMC7_0	QMC7_32	QMC7_64
QMC8	QMC8_0	QMC8_32	QMC8_64
QMC9	QMC9_0	QMC9_32	QMC9_64
QMC10	QMC10_0	QMC10_32	QMC10_64
QMC11	QMC11_0	QMC11_32	QMC11_64
QMC12	QMC12_0	QMC12_32	QMC12_64
QMC13	QMC13_0	QMC13_32	QMC13_64
QMC14	QMC14_0	QMC14_32	QMC14_64
QMC15	QMC15_0	QMC15_32	QMC15_64
QMC16	QMC16_0	QMC16_32	QMC16_64
QMC17	QMC17_0	QMC17_32	QMC17_64
QMC18	QMC18_0	QMC18_32	QMC18_64
QMC19	QMC19_0	QMC19_32	QMC19_64
QMC20	QMC20_0	QMC20_32	QMC20_64
QMC21	QMC21_0	QMC21_32	QMC21_64
QMC22	QMC22_0	QMC22_32	QMC22_64
QMC23	QMC23_0	QMC23_32	QMC23_64
QMC24	QMC24_0	QMC24_32	QMC24_64
QMC25	QMC25_0	QMC25_32	QMC25_64

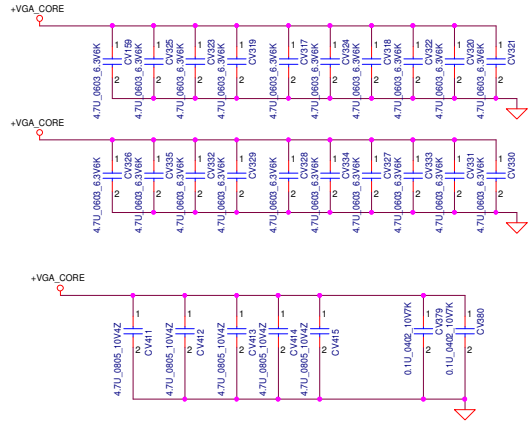
Node F Address	0...31	Node F Address	32...63
QMC1	QMC1_0	QMC1_32	QMC1_64
QMC2	QMC2_0	QMC2_32	QMC2_64
QMC3	QMC3_0	QMC3_32	QMC3_64
QMC4	QMC4_0	QMC4_32	QMC4_64
QMC5	QMC5_0	QMC5_32	QMC5_64
QMC6	QMC6_0	QMC6_32	QMC6_64
QMC7	QMC7_0	QMC7_32	QMC7_64
QMC8	QMC8_0	QMC8_32	QMC8_64
QMC9	QMC9_0	QMC9_32	QMC9_64
QMC10	QMC10_0	QMC10_32	QMC10_64
QMC11	QMC11_0	QMC11_32	QMC11_64
QMC12	QMC12_0	QMC12_32	QMC12_64
QMC13	QMC13_0	QMC13_32	QMC13_64
QMC14	QMC14_0	QMC14_32	QMC14_64
QMC15	QMC15_0	QMC15_32	QMC15_64
QMC16	QMC16_0	QMC16_32	QMC16_64
QMC17	QMC17_0	QMC17_32	QMC17_64
QMC18	QMC18_0	QMC18_32	QMC18_64
QMC19	QMC19_0	QMC19_32	QMC19_64
QMC20	QMC20_0	QMC20_32	QMC20_64
QMC21	QMC21_0	QMC21_32	QMC21_64
QMC22	QMC22_0	QMC22_32	QMC22_64
QMC23	QMC23_0	QMC23_32	QMC23_64
QMC24	QMC24_0	QMC24_32	QMC24_64
QMC25	QMC25_0	QMC25_32	QMC25_64

Security Classification	2014/011	Control Document Date	2014/011
Issued Date	2014/011	Declassified Date	2014/011
LA-8751P			

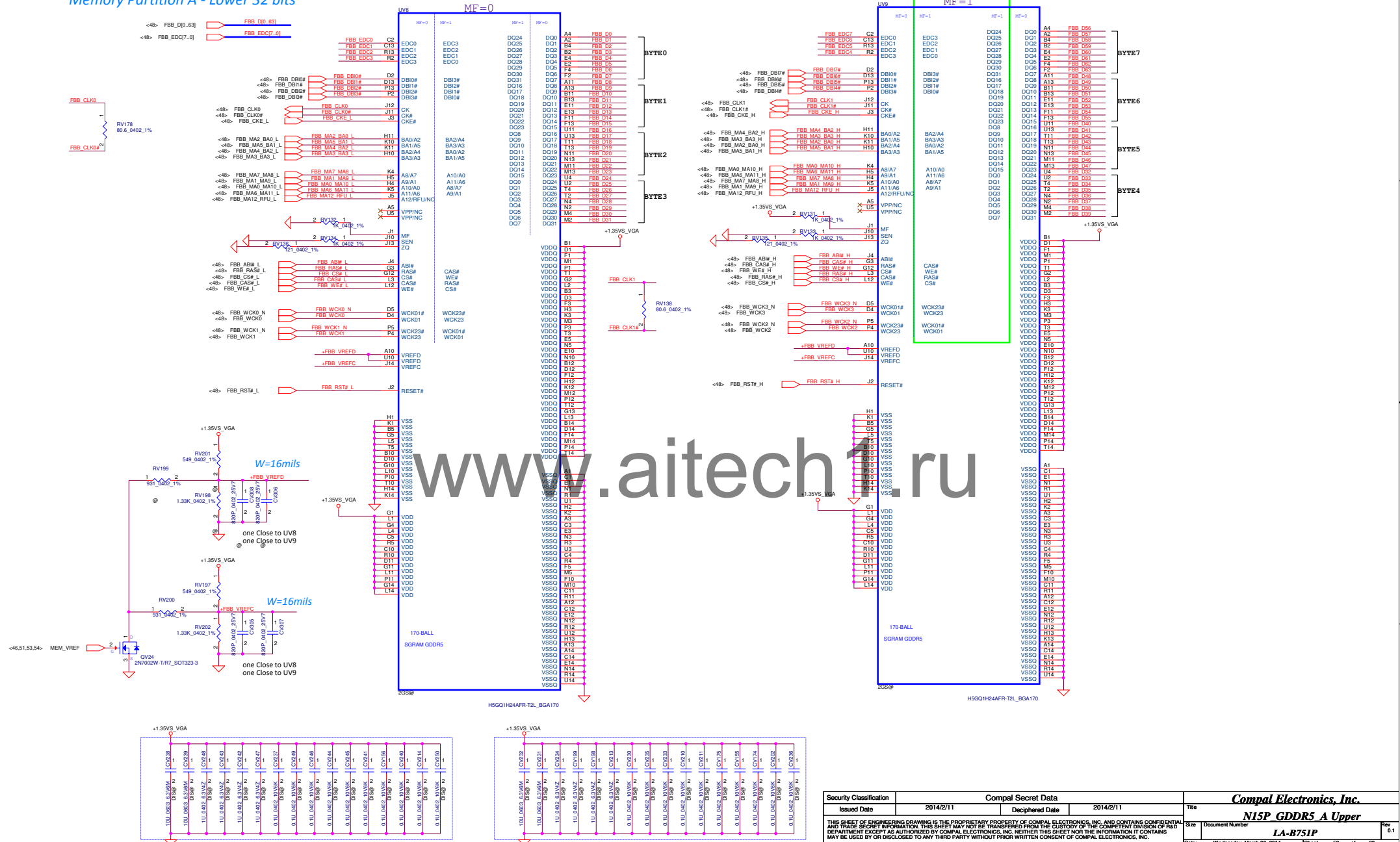




NVDD	22uF	10uF	4.7uF	0.1uF
+VGA_CORE	11	4	40	20



Memory Partition A - Lower 32 bits



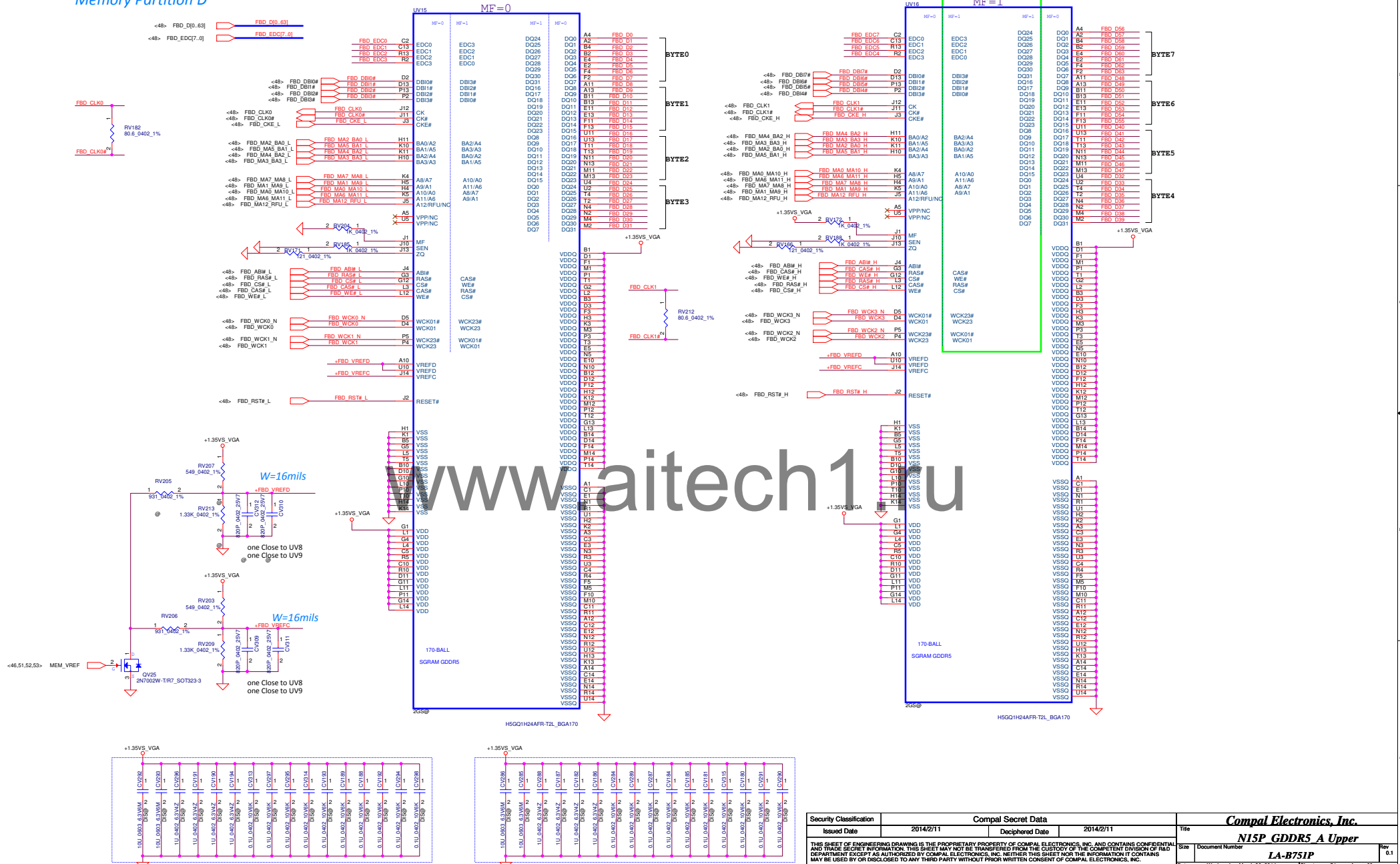
Security Classification	Compal Secret Data		Title	
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Compal Electronics, Inc. N15P GDDRS A Upper
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MF=0

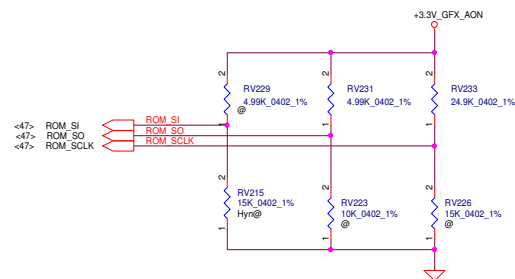
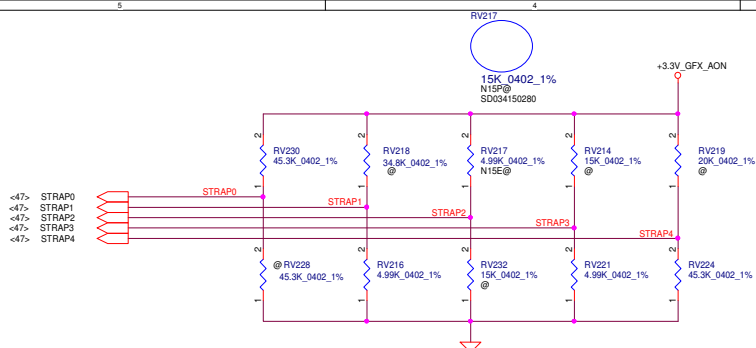


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Memory Partition D



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					LA-B751P 6.1



R_pu



VRAM	Strap	ROM-SI
Hynix H5GC4H24MFR-T2C	0x2	PL 15K
Samsung K4G41325FC-HC04	0x3	PL 20K

Physical Strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDER	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SO	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[4]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_CFG[3]	3GIO_CFG[2]	3GIO_CFG[1]	3GIO_CFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHNAGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	PU to 3V3	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

PCI_DEVID

SUB_VENDER
0- w/o dGPU ROM
1-w/ dGPU ROM

FB[1:0]
0-Reserved
1-Reserved
2-256M
3-Reserved

VGA_DEVICE
0- Non-permyary 3D
1-

SMB_ALT_ADDR
0-0x9E
1-0x9C(Multi-GPU)

PEX_PLL_EN_TERM
0-Disable
1-Enable

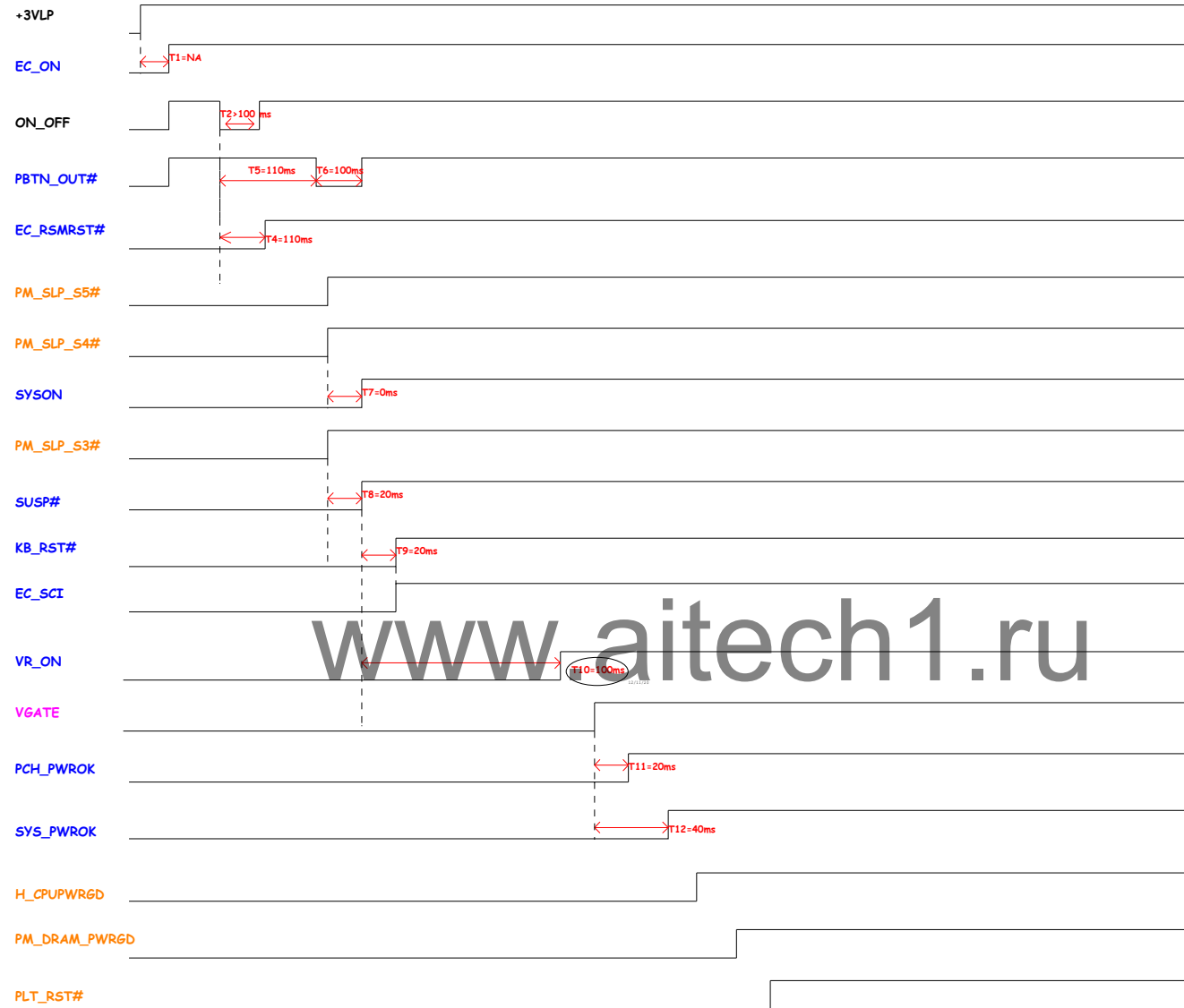
3GIO_PADCFG
0110-GEN1/GEN2
0000-GEN3

PCIE_MAX_SPEED
0-booting to PCIE Gen1
1-booting to PCIE Gen2/Gen3

PCIE_SPEED_CHNAGE_GEN3
0-Disable PCIE Gen3
1-Enable PCIE Gen3

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				Date: Wednesday, March 26, 2014	Sheet 55 of 69

Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
8							
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11							
12							
13							
14							
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39							
40							
41							

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CC = 3A
CV = 17.7V

I_{ada}=0~12.3A (240W)
I_{ada}=0~9.23A (180W)

ADP_I = 40*I_{adapter}*R_{sense}

BATT++

VIN

BAT54CW_SOT323-3

PC707

PC708

PC709

PC710

PC711

PC712

PC713

PC714

PC715

PC716

PC717

PC718

PC719

PC720

PC721

PC722

PC723

PC724

PC725

PC726

PC727

PC728

PC729

PC730

PC731

PC732

PC733

PC734

PC735

PC736

PC737

PC738

PC739

PC740

PC741

PC742

PC743

PC744

PC745

PC746

PC747

PC748

PC749

PC750

PC751

PC752

PC753

PC754

PC755

PC756

PC757

PC758

PC759

PC760

PC761

PC762

PC763

PC764

PC765

PC766

PC767

PC768

PC769

PC770

PC771

PC772

PC773

PC774

PC775

PC776

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PC778

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PC781

PC782

PC783

PC784

PC785

PC786

PC787

PC788

PC789

PC790

PC791

PC792

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PC794

PC795

PC796

PC797

PC798

PC799

PC800

PC801

PC802

PC803

PC804

PC805

PC806

PC807

PC808

PC809

PC810

PC811

PC812

PC813

PC814

PC815

PC816

PC817

PC818

PC819

PC820

PC821

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$$3.3V \times 8.7A = 28.71W$$

$$28.71 / 0.85 / 11 = 3.07A$$

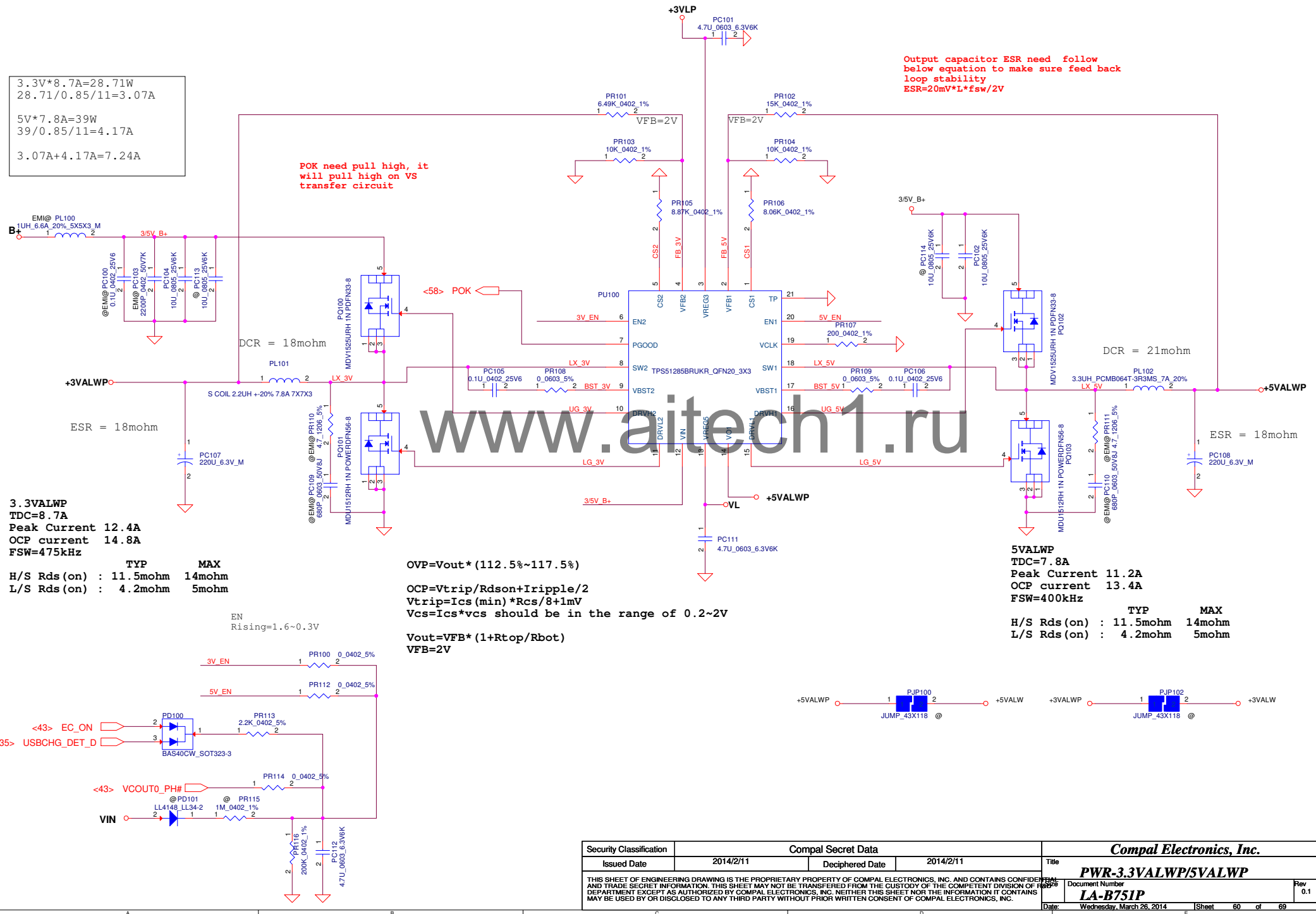
$$5V \times 7.8A = 39W$$

$$39 / 0.85 / 11 = 4.17A$$

$$3.07A + 4.17A = 7.24A$$

POK need pull high, it will pull high on VS transfer circuit

Output capacitor ESR need follow below equation to make sure feed back loop stability
 $ESR = 20mV \times L \times f_{sw} / 2V$



OVP=Vout * (112.5%~117.5%)
 OCP=Vtrip/Rdson+Iripple/2
 Vtrip=Ics(min) * Rcs/8+1mV
 Vcs=Ics*vcs should be in the range of 0.2~2V
 Vout=VFB * (1+Rtop/Rbot)
 VFB=2V

5VALWP
 TDC=7.8A
 Peak Current 11.2A
 OCP current 13.4A
 FSW=400kHz
 H/S Rds(on) : 11.5mohm 14mohm
 L/S Rds(on) : 4.2mohm 5mohm

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$$1.35V \times (7.64A + 1A) = 11.66W$$

$$11.66 / 0.85 / 11 = 1.24A$$

1.35VP
TDC=7.64A
Ipeak=10.92A
OCP=13.1A
Switching Frequency: 285kHz

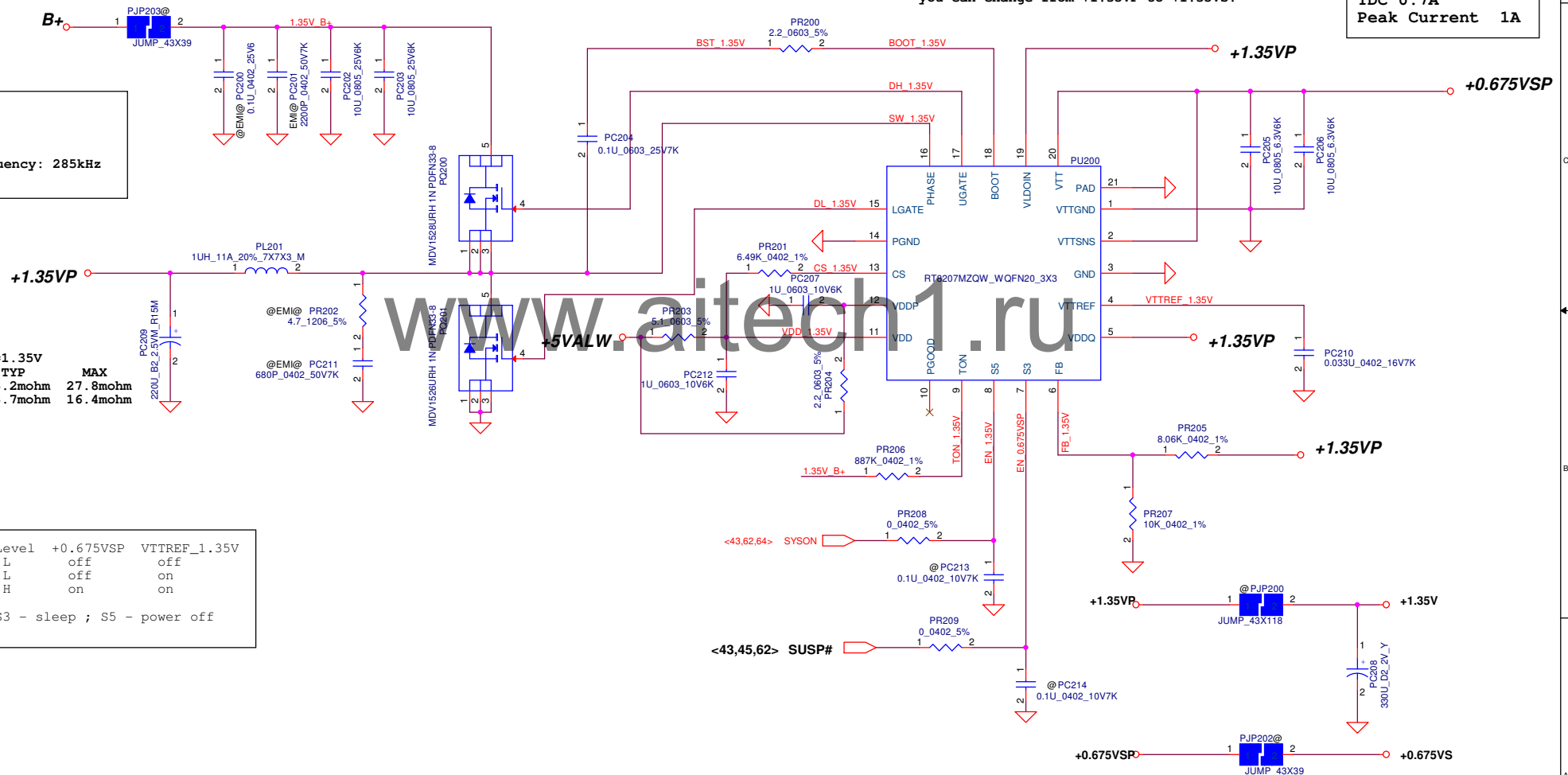
OVP: 110%~120%
VFB=0.75V, Vout=1.35V
TYP MAX
H/S Rds(on) : 23.2mohm 27.8mohm
L/S Rds(on) : 13.7mohm 16.4mohm

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

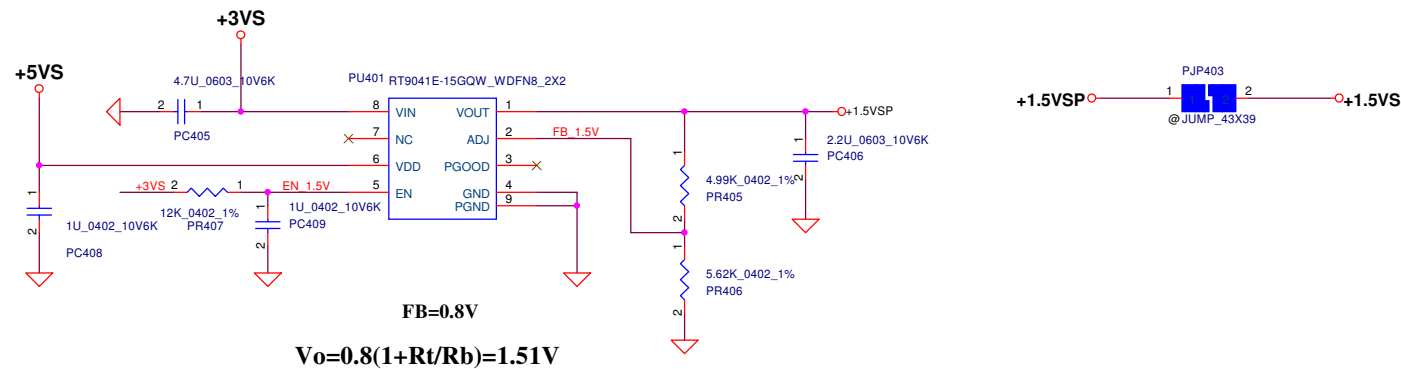
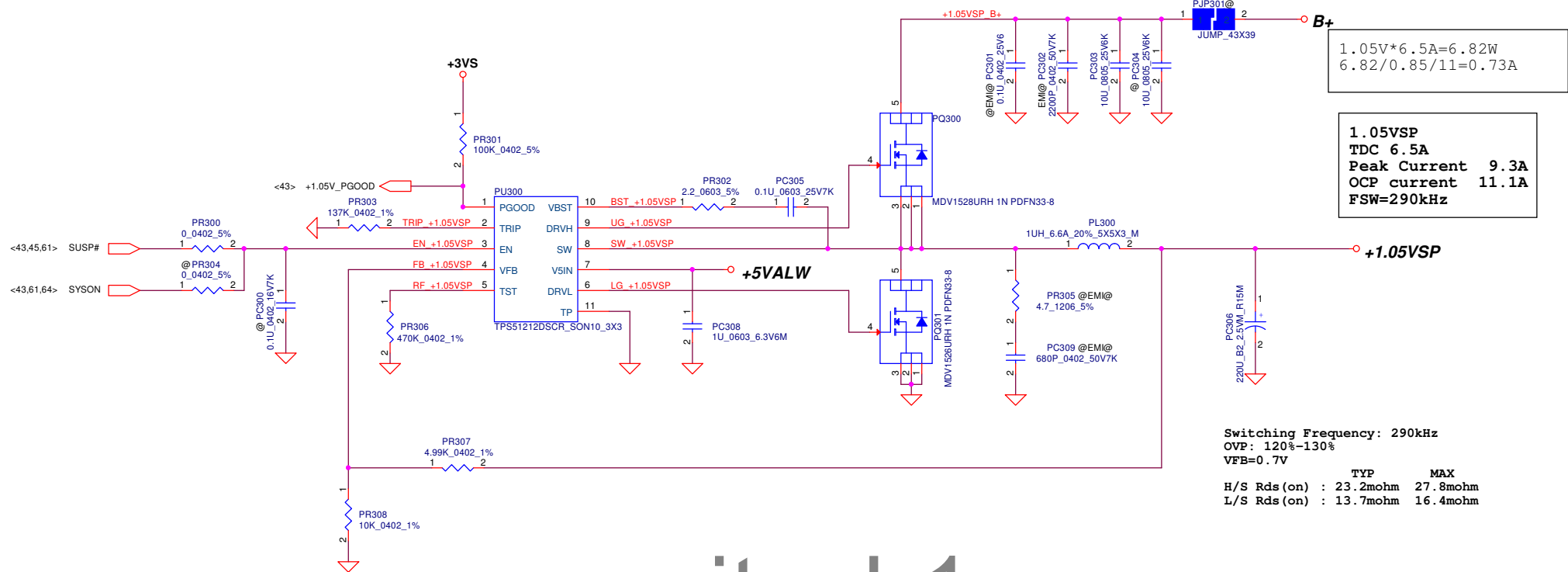
Note: S3 - sleep ; S5 - power off

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675VOLT +/- 5%
TDC 0.7A
Peak Current 1A

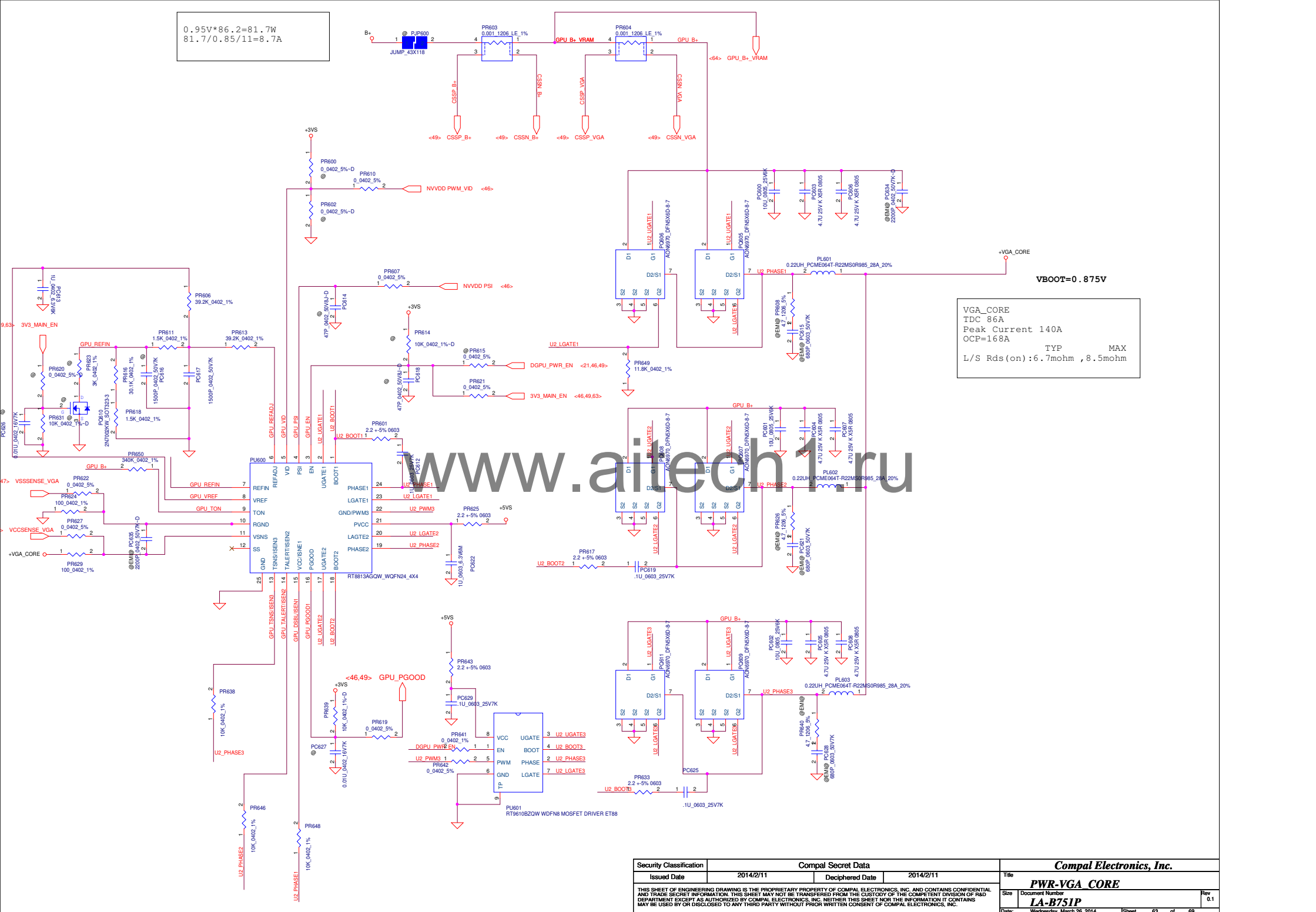


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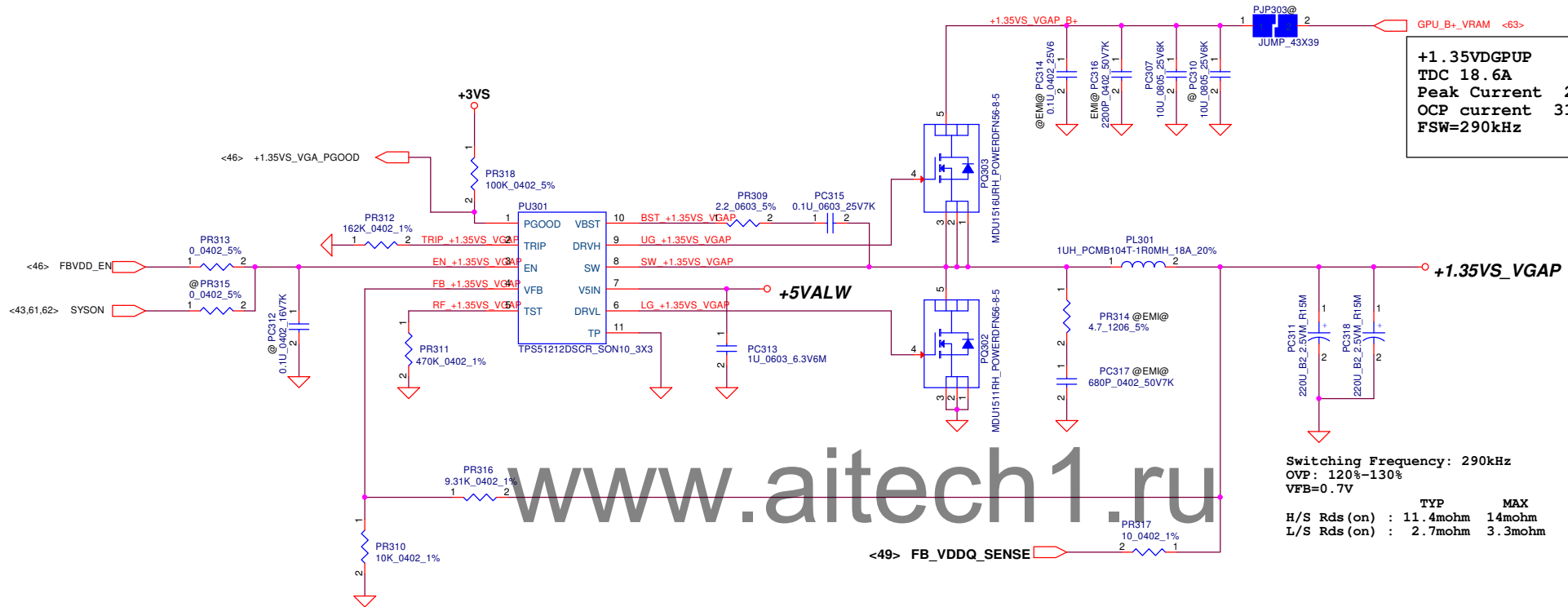
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$0.95V \times 86.2 = 81.7W$
 $81.7 / 0.85 / 11 = 8.7A$



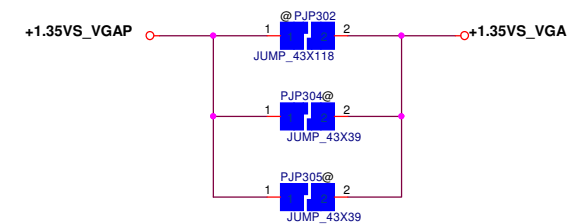
1.35V*18.6A=25.11W
33.42/0.85/11=2.68A

+1.35V DGPUP
TDC 18.6A
Peak Current 26.57A
OCP current 31.88A
FSW=290kHz

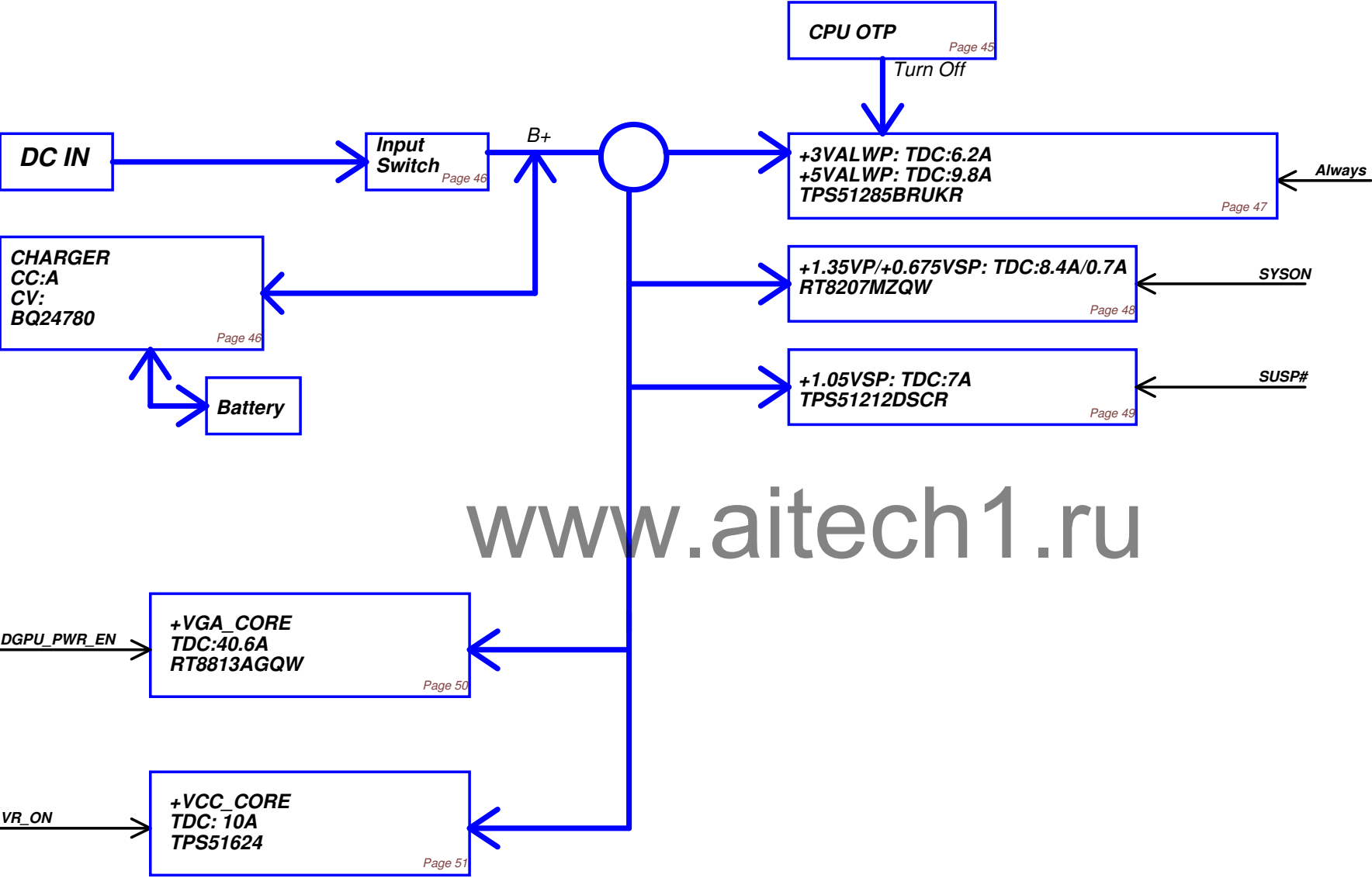


Switching Frequency: 290kHz
OVP: 120%-130%
VFB=0.7V

	TYP	MAX
H/S Rds (on)	11.4mohm	14mohm
L/S Rds (on)	2.7mohm	3.3mohm



Power block



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[illegible]

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